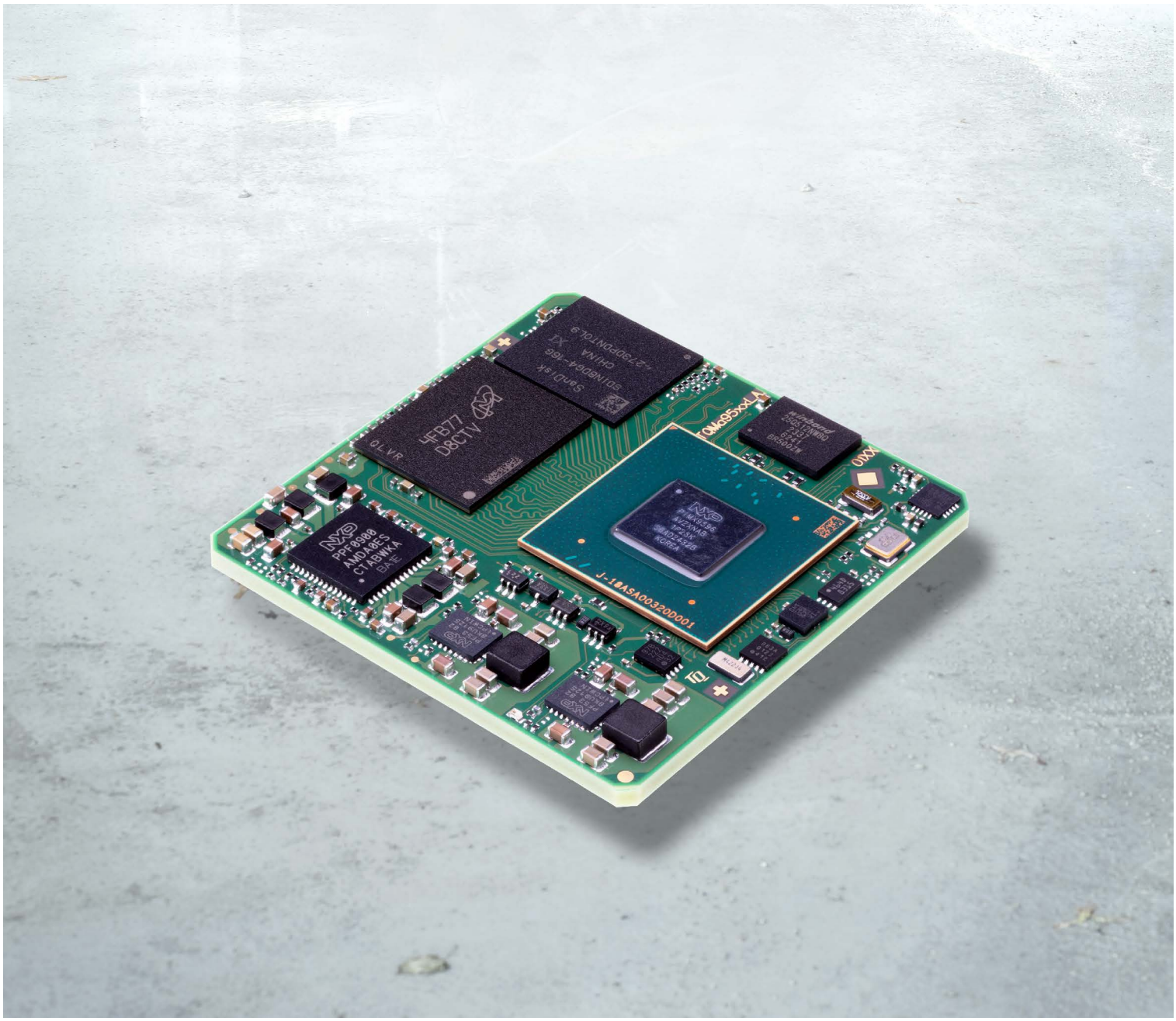
TQMa95xxLA
Preliminary User's Manual

TQMa95xxLA UM 0001
05.11.2024



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	05.11.2024	Kreuzer	All	Initial release

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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa95xxLA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa95xxCA circuit diagram
- MBa95xxCA User's Manual
- i.MX 95 Data Sheet
- i.MX 95 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa95xxLA

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of TQMa95xxLA revision 01xx in combination with the MBa95xxCA and refers to some software settings. The MBa95xxCA serves as an evaluation board for the TQMa95xxLA. A certain TQMa95xxLA derivative does not necessarily provide all features described in this Preliminary User's Manual. This Preliminary User's Manual does also not replace the NXP i.MX 95 Reference Manual (2). The CPU derivatives provide up to six Arm Cortex-A55 cores, Arm Mali GPU, 4K VPU, ISP and ML acceleration NPU.

The TQMa95xxLA is a universal minimodule, based on these NXP ARM® Cortex®-A55 i.MX 95 CPUs, see also Table 3.

An i.MX 95 Cortex®-A55 core typically operates up to 2 GHz.

2.1 Block diagram i.MX 95

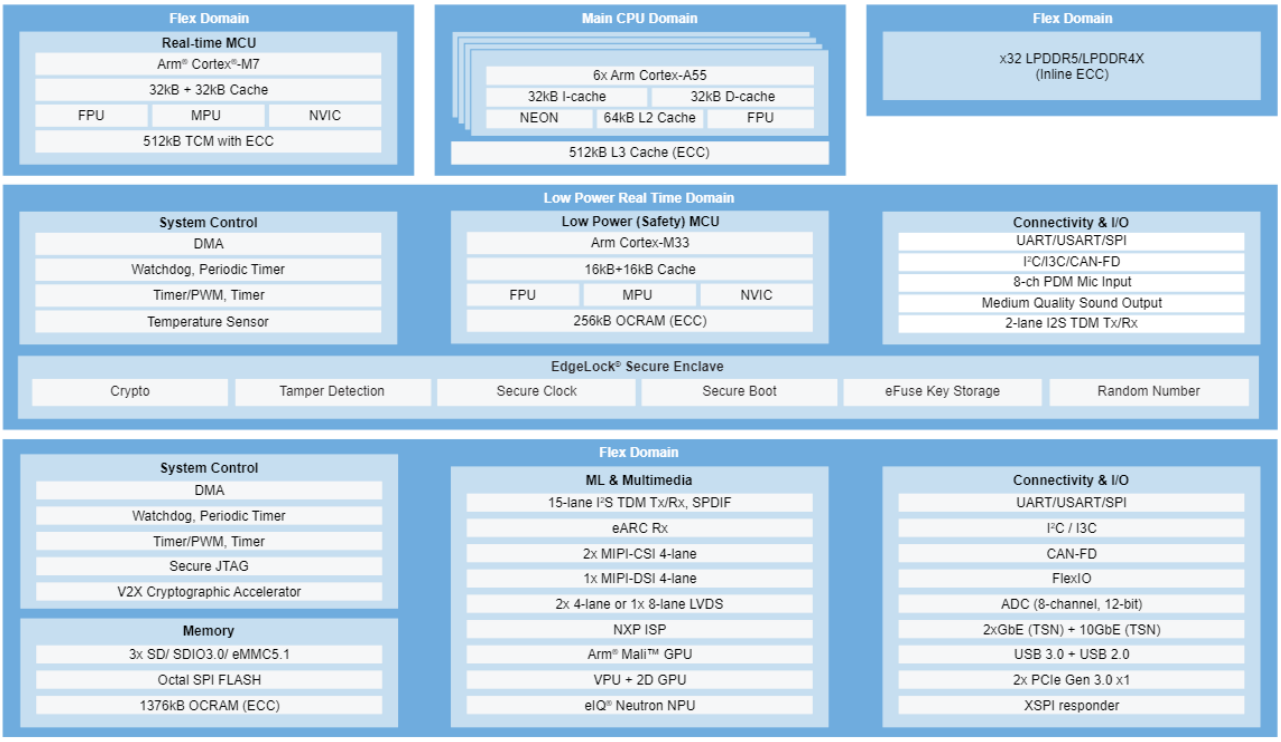

Figure 1: Block diagram i.MX 95 CPU
(Source: NXP)

2.2 Key functions and characteristics

The TQMa95xxLA extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

A suitable i.MX 95 derivative can be selected for each requirement.

The signals are routed to solder pads. All essential components like CPU, LPDDR5 SDRAM, eMMC and power management are already integrated on the TQMa95xxLA. The main features of the TQMa95xxLA are:

- 64-bit NXP i.MX 95 CPU with up to 6× ARM® Cortex®-A55
- x32 RAM in LPDDR5 version
- Quad-SPI NOR flash (optional)
- eMMC (optional)
- Customized EEPROM (optional)
- RTC (optional)
- Plug & Trust Secure Element (optional)
- Gyroscope (optional)

3. ELECTRONICS

The information provided in this Preliminary User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa95xxLA and the BSP provided by TQ-Systems GmbH, see also section 5.

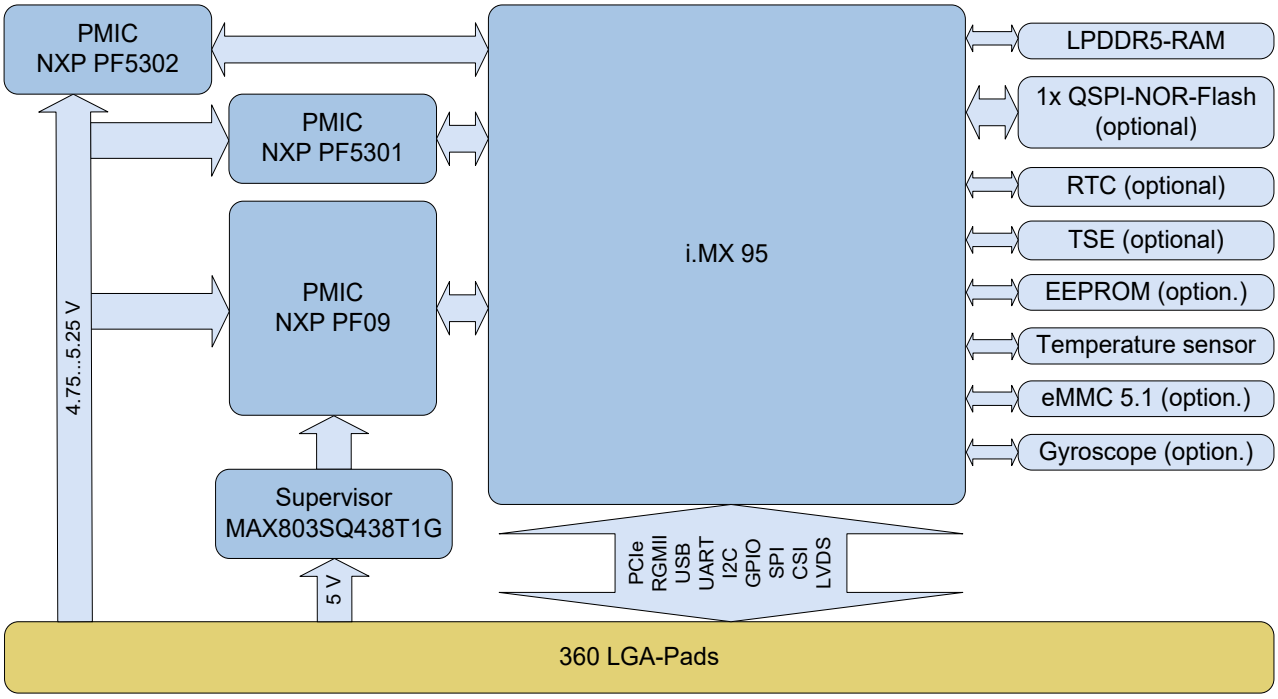

Figure 2: Block diagram TQMa95xxLA

3.1 Interfaces to other systems and devices

Except for the internal interfaces, all functional pins are routed on LGA balls. Each customer must check the suitability of the multiplexing in the respective project and adapt it if necessary.

The following table shows the possible primary interfaces of the TQMa95xxLA that can be muxed simultaneously:

Table 2: Interfaces TQMa95xxLA

i.MX 95 interface	Quantity	Remark
Internal interfaces		
DRAM	1	LPDDR5, x32
FlexSPI (NOR-Flash)	1	Default for QSPI use
USDHC1 (eMMC)	1	8 Bit (HS400)
External interfaces		
ADC	1	8x Inputs
EARC	1	Rx only
GPIO	38	
I2C	2	1x for PMICs, 1x for other peripheries
JTAG	1	
LVDS	2	4x diff. DATA, 1x diff. CLK
MIPI CSI	1	4x diff. DATA, 1x diff. CLK
MIPI CSI / DSI	1	4x diff. DATA, 1x diff. CLK
RGMII	2	
XGMII	1	
PCIe	2	
PDM	1	
SAI	1	
Smartcard ISO14443 / ISO7816	1	optionally provided by TSE
TAMPER	2	
UART	2	
USB	2	USB1 as USB 3.0 and USB2 as USB 2.0
USDHC3	1	4 Bit
SD-Card	1	4 Bit

3.2 Pin multiplexing

When using the CPU signals, the multiple pin configurations by different CPU-internal function units must be taken note of.
The pin assignment listed in Table 3 refers to the corresponding BSP provided by TQ-Systems GmbH in combination with the MBa95xxCA.
The electrical and pin characteristics are to be taken from the i.MX 95 Data Sheet (1), the i.MX 95 Reference Manual (2), and the PMIC Data Sheet (4) .

Attention: Destruction or malfunction	
	Depending on the configuration, many i.MX 95 balls can provide several different functions. Please take note of the information in the i.MX 95 Reference Manual (2), and the i.MX 95 Errata (3) concerning the configuration of these pins before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa95xxLA. The meanings given in the following tables must be observed: RFU: Reserved pins without function. To support future TQMa95xxLA versions, these pins must not be connected. DNC: These pins must not be connected, they have to be left open. A: Indicates an optional interface, implemented on pins shared with another use

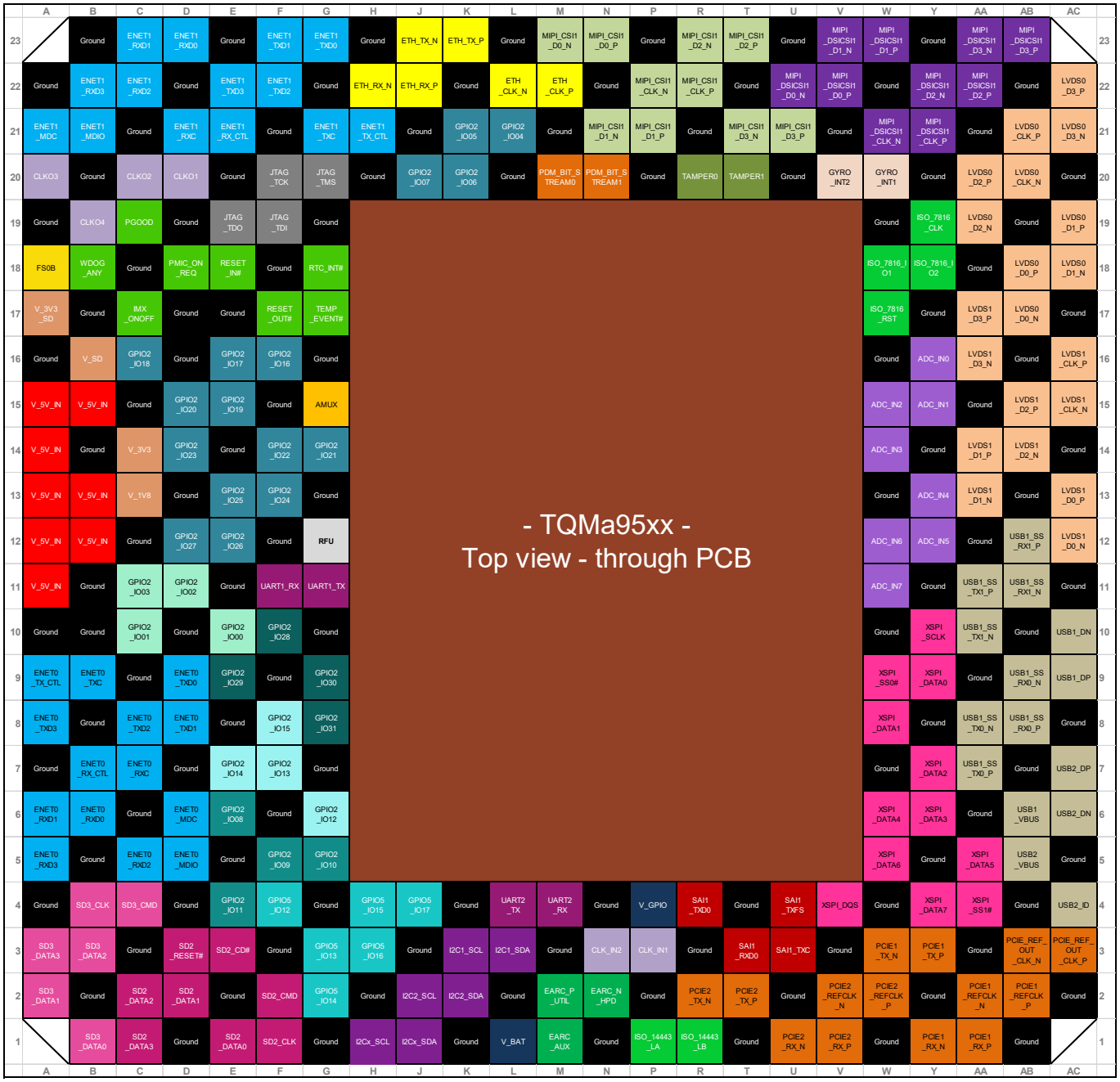

Figure 3: LGA pads layout

3.3 LGA pads

Table 3: Pinout LGA pads

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
A1	-	Not available		-	-	
B1	SD3_DATA0	QSPI	I/O	1.8 V	AG49	
C1	SD2_DATA3	SD-Card	I/O	V_SD	AA49	
D1	Ground	Power	P	0 V	-	
E1	SD2_DATA0	SD-Card	I/O	V_SD	AC51	
F1	SD2_CLK	SD-Card	O	V_SD	AB48	
G1	Ground	Power	P	0 V	-	
H1	I2Cx_SCL	I2C	O	3.3 V	-	
J1	I2Cx_SDA	I2C	I/O	3.3 V	-	
K1	Ground	Power	P	0 V	-	
L1	V_BAT	Power	P	3 V	-	Power input
M1	EARC_AUX	Audio	O	1.8 V	AA45	
N1	Ground	Power	P	0 V	-	
P1	ISO_14443_LA	ISO_14443	I/O	3.3 V	-	
R1	ISO_14443_LB	ISO_14443	I/O	3.3 V	-	
T1	Ground	Power	P	0 V	-	
U1	PCIE2_RX_N	PCIe	I	1.8 V	C35	
V1	PCIE2_RX_P	PCIe	I	1.8 V	B34	
W1	Ground	Power	P	0 V	-	
Y1	PCIE1_RX_N	PCIe	I	1.8 V	A29	
AA1	PCIE1_RX_P	PCIe	I	1.8 V	B28	
AB1	Ground	Power	P	0 V	-	
AC1	-	Not available		-	-	
A2	SD3_DATA1	QSPI	I/O	1.8 V	AH52	
B2	Ground	Power	P	0 V	-	
C2	SD2_DATA2	SD-Card	I/O	V_SD	AA51	
D2	SD2_DATA1	SD-Card	I/O	V_SD	AC49	
E2	Ground	Power	P	0 V	-	
F2	SD2_CMD	SD-Card	I/O	V_SD	AB52	
G2	GPIO5_IO14	GPIO	I/O	V_GPIO	W49	
H2	Ground	Power	P	0 V	-	
J2	I2C2_SCL	I2C	O	3.3 V	E43	
K2	I2C2_SDA	I2C	I/O	3.3 V	E45	
L2	Ground	Power	P	0 V	-	
M2	EARC_P_UTIL	Audio	O	1.8 V	Y44	
N2	EARC_N_HPD	Audio	I	1.8 V	Y46	
P2	Ground	Power	P	0 V	-	
R2	PCIE2_TX_N	PCIe	O	1.8 V	F32	
T2	PCIE2_TX_P	PCIe	O	1.8 V	E31	
U2	Ground	Power	P	0 V	-	
V2	PCIE2_REFCLK_N	PCIe	I	1.8 V	A33	
W2	PCIE2_REFCLK_P	PCIe	I	1.8 V	B32	
Y2	Ground	Power	P	0 V	-	
AA2	PCIE1_REFCLK_N	PCIe	I	1.8 V	C31	
AB2	PCIE1_REFCLK_P	PCIe	I	1.8 V	B30	
AC2	Ground	Power	P	0 V	-	
A3	SD3_DATA3	QSPI	I/O	1.8 V	AF52	
B3	SD3_DATA2	QSPI	I/O	1.8 V	AE49	
C3	Ground	Power	P	0 V	-	
D3	SD2_RESET#	SD-Card	O	V_SD	AD52	
E3	SD2_CD#	SD-Card	I	V_SD	AD48	
F3	Ground	Power	P	0 V	-	
G3	GPIO5_IO13	GPIO	I/O	V_GPIO	W45	
H3	GPIO5_IO16	GPIO	I/O	V_GPIO	Y48	

LGA pads (continued)

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
J3	Ground	Power	P	0 V	-	
K3	I2C1_SCL	I2C	O	3.3 V	D48	3V3 pull-up resistors on module
L3	I2C1_SDA	I2C	I/O	3.3 V	D52	3V3 pull-up resistors on module
M3	Ground	Power	P	0 V	-	
N3	CLK_IN2	CLK	I	1.8 V	E39	
P3	CLK_IN1	CLK	I	1.8 V	E37	
R3	Ground	Power	P	0 V	-	
T3	SAI1_RXD0	SAI	I	3.3 V	H52	
U3	SAI1_TXC	SAI	O	3.3 V	G51	
V3	Ground	Power	P	0 V	-	
W3	PCIE1_TX_N	PCIe	O	1.8 V	D30	
Y3	PCIE1_TX_P	PCIe	O	1.8 V	E29	
AA3	Ground	Power	P	0 V	-	
AB3	PCIE_REF_OUT_CLK_N	PCIe	O	1.8 V	C27	
AC3	PCIE_REF_OUT_CLK_P	PCIe	O	1.8 V	B26	
A4	Ground	Power	P	0 V	-	
B4	SD3_CLK	QSPI	O	1.8 V	AG51	
C4	SD3_CMD	QSPI	I/O	1.8 V	AF48	
D4	Ground	Power	P	0 V	-	
E4	GPIO2_IO11	GPIO	I/O	V_GPIO	M52	
F4	GPIO5_IO12	GPIO	I/O	V_GPIO	V52	
G4	Ground	Power	P	0 V	-	
H4	GPIO5_IO15	GPIO	I/O	V_GPIO	W51	
J4	GPIO5_IO17	GPIO	I/O	V_GPIO	Y52	
K4	Ground	Power	P	0 V	-	
L4	UART2_TX	UART	O	3.3 V	F48	Used as BOOT_MODE1 at startup
M4	UART2_RX	UART	I	3.3 V	E51	
N4	Ground	Power	P	0 V	-	
P4	V_GPIO	Power	P	1.8 / 3.3 V	T40, U41	Power input
R4	SAI1_TXD0	SAI	O	3.3 V	H48	Used as BOOT_MODE3 at startup
T4	Ground	Power	P	0 V	-	
U4	SAI1_TXFS	SAI	O	3.3 V	G49	Used as BOOT_MODE2 at startup
V4	XSPI_DQS	XSPI	O	1.8 V	AK44	
W4	Ground	Power	P	0 V	-	
Y4	XSPI_DATA7	XSPI	I/O	1.8 V	AH50	
AA4	XSPI_SS1#	XSPI	O	1.8 V	AH42	
AB4	Ground	Power	P	0 V	-	
AC4	USB2_ID	USB	I	1.8 V	F24	
A5	ENET0_RXD3	ENET	I	1.8 V	AH38	
B5	Ground	Power	P	0 V	-	
C5	ENET0_RXD2	ENET	I	1.8 V	AJ37	
D5	ENET0_MDIO	ENET	I/O	1.8 V	AJ39	
E5	Ground	Power	P	0 V	-	
F5	GPIO2_IO09	GPIO	I/O	V_GPIO	M46	
G5	GPIO2_IO10	GPIO	I/O	V_GPIO	M48	
H5, J5, K5, L5, M5, N5, P5, R5, T5, U5, V5		Not available		-	-	-
W5	XSPI_DATA6	XSPI	I/O	1.8 V	AJ51	
Y5	Ground	Power	P	0 V	-	
AA5	XSPI_DATA5	XSPI	I/O	1.8 V	AK50	
AB5	USB2_VBUS	USB	P	5 V	E27	
AC5	Ground	Power	P	0 V	-	
A6	ENET0_RXD1	ENET	I	1.8 V	AK36	
B6	ENET0_RXD0	ENET	I	1.8 V	AJ35	
C6	Ground	Power	P	0 V	-	

LGA pads (continued)

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
D6	ENET0_MDC	ENET	O	1.8 V	AK40	
E6	GPIO2_IO08	GPIO	I/O	V_GPIO	M44	
F6	Ground	Power	P	0 V	-	
G6	GPIO2_IO12	GPIO	I/O	V_GPIO	N45	
H6, J6, K6, L6, M6, N6, P6, R6, T6, U6, V6	Not available	-	-	-		
W6	XSPI_DATA4	XSPI	I/O	1.8 V	AJ49	
Y6	XSPI_DATA3	XSPI	I/O	1.8 V	AK48	Not usable if module contains NOR-Flash
AA6	Ground	Power	P	0 V	-	
AB6	USB1_VBUS	USB	P	5 V	E23	
AC6	USB2_DN	USB	I/O	3.3 V	A25	
A7	Ground	Power	P	0 V	-	
B7	ENET0_RX_CTL	ENET	I	1.8 V	AH34	
C7	ENET0_RXC	ENET	I	1.8 V	AJ33	
D7	Ground	Power	P	0 V	-	
E7	GPIO2_IO14	Config	I/O	V_GPIO	N51	
F7	GPIO2_IO13	Config	I/O	V_GPIO	N49	
G7	Ground	Power	P	0 V	-	
H7, J7, K7, L7, M7, N7, P7, R7, T7, U7, V7	Not available	-	-	-		
W7	Ground	Power	P	0 V	-	
Y7	XSPI_DATA2	XSPI	I/O	1.8 V	AJ47	Not usable if module contains NOR-Flash
AA7	USB1_SS_TX0_P	USB	O	0.8 V	D26	
AB7	Ground	Power	P	0 V	-	
AC7	USB2_DP	USB	I/O	3.3 V	B24	
A8	ENET0_TXD3	ENET	O	1.8 V	AG37	
B8	Ground	Power	P	0 V	-	
C8	ENET0_TXD2	ENET	O	1.8 V	AF36	
D8	ENET0_TXD1	ENET	O	1.8 V	AG35	
E8	Ground	Power	P	0 V	-	
F8	GPIO2_IO15	GPIO	I/O	V_GPIO	P44	
G8	GPIO2_IO31	GPIO	I/O	V_GPIO	V48	
H8, J8, K8, L8, M8, N8, P8, R8, T8, U8, V8	Not available	-	-	-		
W8	XSPI_DATA1	XSPI	I/O	1.8 V	AH46	Not usable if module contains NOR-Flash
Y8	Ground	Power	P	0 V	-	
AA8	USB1_SS_TX0_N	USB	O	0.8 V	E25	
AB8	USB1_SS_RX0_P	USB	I	0.8 V	A21	
AC8	Ground	Power	P	0 V	-	
A9	ENET0_TX_CTL	ENET	O	1.8 V	AF32	
B9	ENET0_TXC	ENET	O	1.8 V	AG31	
C9	Ground	Power	P	0 V	-	
D9	ENET0_TXD0	ENET	O	1.8 V	AG33	
E9	GPIO2_IO29	GPIO	I/O	V_GPIO	V44	
F9	Ground	Power	P	0 V	-	
G9	GPIO2_IO30	GPIO	I/O	V_GPIO	V46	
H9, J9, K9, L9, M9, N9, P9, R9, T9, U9, V9	Not available	-	-	-		
W9	XSPI_SS0#	XSPI	O	1.8 V	AJ41	Not usable if module contains NOR-Flash
Y9	XSPI_DATA0	XSPI	I/O	1.8 V	AJ45	Not usable if module contains NOR-Flash
AA9	Ground	Power	P	0 V	-	
AB9	USB1_SS_RX0_N	USB	I	0.8 V	B20	
AC9	USB1_DP	USB	I/O	3.3 V	C19	
A10	Ground	Power	P	0 V	-	

LGA pads (continued)

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
B10	Ground	Power	P	0 V	-	
C10	GPIO2_IO01	GPIO	I/O	V_GPIO	J51	
D10	Ground	Power	P	0 V	-	
E10	GPIO2_IO00	GPIO	I/O	V_GPIO	J49	
F10	GPIO2_IO28	GPIO	I/O	V_GPIO	U51	
G10	Ground	Power	P	0 V	-	
H10, J10, K10, L10, M10, N10, P10, R10, T10, U10, V10		Not available		-	-	-
W10	Ground	Power	P	0 V	-	
Y10	XSPI_SCLK	XSPI	O	1.8 V	AJ43	
AA10	USB1_SS_TX1_N	USB	O	0.8 V	D22	
AB10	Ground	Power	P	0 V	-	
AC10	USB1_DN	USB	I/O	3.3 V	B18	
A11	V_5V_IN	Power	P	5 V	-	Power input
B11	Ground	Power	P	0 V	-	
C11	GPIO2_IO03	GPIO	I/O	V_GPIO	K52	
D11	GPIO2_IO02	GPIO	I/O	V_GPIO	K48	
E11	Ground	Power	P	0 V	-	
F11	UART1_RX	UART	I	3.3 V	E49	
G11	UART1_TX	UART	O	3.3 V	F52	Used as BOOT_MODE0 at startup
H11, J11, K11, L11, M11, N11, P11, R11, T11, U11, V11		Not available		-	-	-
W11	ADC_IN7	ADC	I	1.8 V	A45	
Y11	Ground	Power	P	0 V	-	
AA11	USB1_SS_TX1_P	USB	O	0.8 V	E21	
AB11	USB1_SS_RX1_N	USB	I	0.8 V	A17	
AC11	Ground	Power	P	0 V	-	
A12	V_5V_IN	Power	P	5 V	-	Power input
B12	V_5V_IN	Power	P	5 V	-	Power input
C12	Ground	Power	P	0 V	-	
D12	GPIO2_IO27	GPIO	I/O	V_GPIO	U49	
E12	GPIO2_IO26	GPIO	I/O	V_GPIO	U45	
F12	Ground	Power	P	0 V	-	
G12	**RFU**	-	-	-	-	
H12, J12, K12, L12, M12, N12, P12, R12, T12, U12, V12		Not available		-	-	-
W12	ADC_IN6	ADC	I	1.8 V	B44	
Y12	ADC_IN5	ADC	I	1.8 V	B42	
AA12	Ground	Power	P	0 V	-	
AB12	USB1_SS_RX1_P	USB	I	0.8 V	B16	
AC12	LVDS1_D0_N	LVDS	O	1.8 V	A3	
A13	V_5V_IN	Power	P	5 V	-	Power input
B13	V_5V_IN	Power	P	5 V	-	Power input
C13	V_1V8	Power	P	1.8 V	-	Power output (max. 500 mA)
D13	Ground	Power	P	0 V	-	
E13	GPIO2_IO25	GPIO	I/O	V_GPIO	T52	
F13	GPIO2_IO24	GPIO	I/O	V_GPIO	T48	
G13	Ground	Power	P	0 V	-	
H13, J13, K13, L13, M13, N13, P13, R13, T13, U13, V13		Not available		-	-	-
W13	Ground	Power	P	0 V	-	
Y13	ADC_IN4	ADC	I	1.8 V	A41	
AA13	LVDS1_D1_N	LVDS	O	1.8 V	C3	
AB13	Ground	Power	P	0 V	-	

LGA pads (continued)

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
AC13	LVDS1_D0_P	LVDS	O	1.8 V	B2	
A14	V_5V_IN	Power	P	5 V	-	Power input
B14	Ground	Power	P	0 V	-	
C14	V_3V3	Power	P	3.3 V	-	Power output (max. 500 mA)
D14	GPIO2_IO23	GPIO	I/O	V_GPIO	T46	
E14	Ground	Power	P	0 V	-	
F14	GPIO2_IO22	GPIO	I/O	V_GPIO	T44	
G14	GPIO2_IO21	GPIO	I/O	V_GPIO	R51	
H14, J14, K14, L14, M14, N14, P14, R14, T14, U14, V14		Not available		-	-	-
W14	ADC_IN3	ADC	I	1.8 V	B40	
Y14	Ground	Power	P	0 V	-	
AA14	LVDS1_D1_P	LVDS	O	1.8 V	C1	
AB14	LVDS1_D2_N	LVDS	O	1.8 V	E3	
AC14	Ground	Power	P	0 V	-	
A15	V_5V_IN	Power	P	5 V	-	Power input
B15	V_5V_IN	Power	P	5 V	-	Power input
C15	Ground	Power	P	0 V	-	
D15	GPIO2_IO20	GPIO	I/O	V_GPIO	R49	
E15	GPIO2_IO19	GPIO	I/O	V_GPIO	R45	
F15	Ground	Power	P	0 V	-	
G15	AMUX	Config	O	1.65 V	-	PMIC status pin - leave unconnected
H15, J15, K15, L15, M15, N15, P15, R15, T15, U15, V15		Not available		-	-	-
W15	ADC_IN2	ADC	I	1.8 V	C39	
Y15	ADC_IN1	ADC	I	1.8 V	B38	
AA15	Ground	Power	P	0 V	-	
AB15	LVDS1_D2_P	LVDS	O	1.8 V	E1	
AC15	LVDS1_CLK_N	LVDS	O	1.8 V	D4	
A16	Ground	Power	P	0 V	-	
B16	V_SD	Power	P	1.8 / 3.3 V	AD36, AD38	Power output (max. 75 mA)
C16	GPIO2_IO18	GPIO	I/O	V_GPIO	P52	
D16	Ground	Power	P	0 V	-	
E16	GPIO2_IO17	GPIO	I/O	V_GPIO	P48	
F16	GPIO2_IO16	GPIO	I/O	V_GPIO	P46	
G16	Ground	Power	P	0 V	-	
H16, J16, K16, L16, M16, N16, P16, R16, T16, U16, V16		Not available		-	-	-
W16	Ground	Power	P	0 V	-	
Y16	ADC_IN0	ADC	I	1.8 V	A37	
AA16	LVDS1_D3_N	LVDS	O	1.8 V	F4	
AB16	Ground	Power	P	0 V	-	
AC16	LVDS1_CLK_P	LVDS	O	1.8 V	D2	
A17	V_3V3_SD	Power	P	3.3 V	-	Power output (max. 400 mA)
B17	Ground	Power	P	0 V	-	
C17	IMX_ONOFF	Config	I	1.8 V	F40	
D17	Ground	Power	P	0 V	-	
E17	Ground	Power	P	0 V	-	
F17	RESET_OUT#	Config	O	OD	D42	Open drain (up to 5.5 V)
G17	TEMP_EVENT#	Config	O	OD	-	Open drain (0.9 V to 3.6 V)
H17, J17, K17, L17, M17, N17, P17, R17, T17, U17, V17		Not available		-	-	-

LGA pads (continued)

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
W17	ISO_7816_RST	ISO_7816	I	3.3 V	-	
Y17	Ground	Power	P	0 V	-	
AA17	LVDS1_D3_P	LVDS	O	1.8 V	F2	
AB17	LVDS0_D0_N	LVDS	O	1.8 V	G9	
AC17	Ground	Power	P	0 V	-	
A18	FS0B	Config	O	OD	-	3V3 pull-up resistor on module
B18	WDOG_ANY	GPIO	I/O	3.3 V	J45	I/O behaviour dependent on PMIC model
C18	Ground	Power	P	0 V	-	
D18	PMIC_ON_REQ	Config	I	1.8 V	D44	
E18	RESET_IN#	Config	I	OD	D42	Open drain (1.8 V or higher)
F18	Ground	Power	P	0 V	-	
G18	RTC_INT#	Config	O	OD	-	Open drain (0,7 V to 5,5 V)
H18, J18, K18, L18, M18, N18, P18, R18, T18, U18, V18	Not available			–	–	–
W18	ISO_7816_IO1	ISO_7816	I/O	3.3 V	-	
Y18	ISO_7816_IO2	ISO_7816	I/O	3.3 V	-	
AA18	Ground	Power	P	0 V	-	
AB18	LVDS0_D0_P	LVDS	O	1.8 V	G7	
AC18	LVDS0_D1_N	LVDS	O	1.8 V	F8	
A19	Ground	Power	P	0 V	-	
B19	CLKO4	CLK	O	1.8 V	AJ21	
C19	PGOOD	Config	O	OD	-	3V3 pull-up resistor on module
D19	Ground	Power	P	0 V	-	
E19	JTAG_TDO	JTAG	O	1.8 V	AJ23	
F19	JTAG_TDI	JTAG	I	1.8 V	AK24	
G19	Ground	Power	P	0 V	-	
H19, J19, K19, L19, M19, N19, P19, R19, T19, U19, V19	Not available			–	–	–
W19	Ground	Power	P	0 V	-	
Y19	ISO_7816_CLK	ISO_7816	I	3.3 V	-	
AA19	LVDS0_D2_N	LVDS	O	1.8 V	E7	
AB19	Ground	Power	P	0 V	-	
AC19	LVDS0_D1_P	LVDS	O	1.8 V	F6	
A20	CLKO3	CLK	O	1.8 V	AK20	
B20	Ground	Power	P	0 V	-	
C20	CLKO2	CLK	O	1.8 V	AF20	
D20	CLKO1	CLK	O	1.8 V	AH20	
E20	Ground	Power	P	0 V	-	
F20	JTAG_TCK	JTAG	I	1.8 V	AG21	
G20	JTAG_TMS	JTAG	I	1.8 V	AH22	
H20	Ground	Power	P	0 V	-	
J20	GPIO2_IO07	GPIO	I/O	V_GPIO	L51	
K20	GPIO2_IO06	GPIO	I/O	V_GPIO	L49	
L20	Ground	Power	P	0 V	-	
M20	PDM_BIT_STREAM0	PDM	I	3.3 V	G45	
N20	PDM_BIT_STREAM1	PDM	I	3.3 V	H46	Non maskable interrupt of M33
P20	Ground	Power	P	0 V	-	
R20	TAMPER0	Tamper	I/O	1.8 V	F36	
T20	TAMPER1	Tamper	I/O	1.8 V	D38	
U20	Ground	Power	P	0 V	-	
V20	GYRO_INT2	Config	O	OD / PP	-	Open drain or Push-Pull/active high or low
W20	GYRO_INT1	Config	O	OD / PP	-	Open drain or Push-Pull/active high or low

LGA pads (continued)

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
Y20	Ground	Power	P	0 V	-	
AA20	LVDS0_D2_P	LVDS	O	1.8 V	D6	
AB20	LVDS0_CLK_N	LVDS	O	1.8 V	A5	
AC20	Ground	Power	P	0 V	-	
A21	ENET1_MDC	ENET	O	1.8 V	AK32	
B21	ENET1_MDIO	ENET	I/O	1.8 V	AJ31	
C21	Ground	Power	P	0 V	-	
D21	ENET1_RXC	ENET	I	1.8 V	AJ25	
E21	ENET1_RX_CTL	ENET	I	1.8 V	AH26	
F21	Ground	Power	P	0 V	-	
G21	ENET1_TXC	ENET	O	1.8 V	AG23	
H21	ENET1_TX_CTL	ENET	O	1.8 V	AF24	
J21	Ground	Power	P	0 V	-	
K21	GPIO2_IO05	GPIO	I/O	V_GPIO	L45	
L21	GPIO2_IO04	GPIO	I/O	V_GPIO	K46	
M21	Ground	Power	P	0 V	-	
N21	MIPI_CSI1_D1_N	MIPI_CSI	I	1.8 V	D18	
P21	MIPI_CSI1_D1_P	MIPI_CSI	I	1.8 V	E17	
R21	Ground	Power	P	0 V	-	
T21	MIPI_CSI1_D3_N	MIPI_CSI	I	1.8 V	F12	
U21	MIPI_CSI1_D3_P	MIPI_CSI	I	1.8 V	E11	
V21	Ground	Power	P	0 V	-	
W21	MIPI_DSICSI1_CLK_N	MIPI_DSICSI	I/O	1.8 V	C11	
Y21	MIPI_DSICSI1_CLK_P	MIPI_DSICSI	I/O	1.8 V	B10	
AA21	Ground	Power	P	0 V	-	
AB21	LVDS0_CLK_P	LVDS	O	1.8 V	B4	
AC21	LVDS0_D3_N	LVDS	O	1.8 V	E9	
A22	Ground	Power	P	0 V	-	
B22	ENET1_RXD3	ENET	I	1.8 V	AH30	
C22	ENET1_RXD2	ENET	I	1.8 V	AJ29	
D22	Ground	Power	P	0 V	-	
E22	ENET1_TXD3	ENET	O	1.8 V	AG29	
F22	ENET1_TXD2	ENET	O	1.8 V	AF28	
G22	Ground	Power	P	0 V	-	
H22	ETH_RX_N	ETH	I	0.8 V	AK12	
J22	ETH_RX_P	ETH	I	0.8 V	AJ13	
K22	Ground	Power	P	0 V	-	
L22	ETH_CLK_N	ETH	I/O	0.8 V	AF14	
M22	ETH_CLK_P	ETH	I/O	0.8 V	AG15	
N22	Ground	Power	P	0 V	-	
P22	MIPI_CSI1_CLK_N	MIPI_CSI	I	1.8 V	F16	
R22	MIPI_CSI1_CLK_P	MIPI_CSI	I	1.8 V	E15	
T22	Ground	Power	P	0 V	-	
U22	MIPI_DSICSI1_D0_N	MIPI_DSICSI	I/O	1.8 V	C15	
V22	MIPI_DSICSI1_D0_P	MIPI_DSICSI	I/O	1.8 V	B14	
W22	Ground	Power	P	0 V	-	
Y22	MIPI_DSICSI1_D2_N	MIPI_DSICSI	I/O	1.8 V	A9	
AA22	MIPI_DSICSI1_D2_P	MIPI_DSICSI	I/O	1.8 V	B8	
AB22	Ground	Power	P	0 V	-	
AC22	LVDS0_D3_P	LVDS	O	1.8 V	D8	

LGA pads (continued)

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
A23	-	Not available		-	-	
B23	Ground	Power	P	0 V	-	
C23	ENET1_RXD1	ENET	I	1.8 V	AK28	
D23	ENET1_RXD0	ENET	I	1.8 V	AJ27	
E23	Ground	Power	P	0 V	-	
F23	ENET1_TXD1	ENET	O	1.8 V	AG27	
G23	ENET1_TXD0	ENET	O	1.8 V	AG25	
H23	Ground	Power	P	0 V	-	
J23	ETH_TX_N	ETH	O	0.8 V	AK16	
K23	ETH_TX_P	ETH	O	0.8 V	AJ17	
L23	Ground	Power	P	0 V	-	
M23	MIPI_CSI1_D0_N	MIPI_CSI	I	1.8 V	F20	
N23	MIPI_CSI1_D0_P	MIPI_CSI	I	1.8 V	E19	
P23	Ground	Power	P	0 V	-	
R23	MIPI_CSI1_D2_N	MIPI_CSI	I	1.8 V	D14	
T23	MIPI_CSI1_D2_P	MIPI_CSI	I	1.8 V	E13	
U23	Ground	Power	P	0 V	-	
V23	MIPI_DSICSI1_D1_N	MIPI_DSICSI	I/O	1.8 V	A13	
W23	MIPI_DSICSI1_D1_P	MIPI_DSICSI	I/O	1.8 V	B12	
Y23	Ground	Power	P	0 V	-	
AA23	MIPI_DSICSI1_D3_N	MIPI_DSICSI	I/O	1.8 V	C7	
AB23	MIPI_DSICSI1_D3_P	MIPI_DSICSI	I/O	1.8 V	B6	
AC23	-	Not available		-	-	

The pin assignment listed in Table 3 refers to the corresponding BSP provided by TQ-Systems GmbH.
For information regarding I/O pins in Table 3 refer to the i.MX 95 Data Sheet (1).

3.4 i.MX 95 CPU

3.4.1 i.MX 95 derivatives

Depending on the TQMa95xxLA version, one of the following i.MX 95 derivatives is assembled.

Table 4: i.MX 95 derivatives

TQMa95xxLA variant	CPU derivative	Cortex®-A55 clock	Cortex®-M33 clock	T_J, temperature range
TQMa9554LA-AA	i.MX9554	4 x 1.8 GHz	250 MHz	800 MHz
TQMa9556LA-AA	i.MX9556	6 x 1.8 GHz	250 MHz	800 MHz
TQMa9594LA-AA	i.MX9594	4 x 1.8 GHz	250 MHz	800 MHz
TQMa9596LA-AA	i.MX9596	6 x 1.8 GHz	250 MHz	800 MHz

3.4.2 i.MX 95 errata

Attention: Malfunction	
	Please take note of the current i.MX 95 errata (3).

3.4.3 Boot modes

After the release of IMX_POR# the system controller (SCU) boots from the internal ROM. Depending on the OPT fuses (eFuse) and the boot mode settings of the system controller the system boots from the selected boot source. The following interfaces are available as boot source:

- eMMC
- QSPI-NOR Flash
- Serial downloader
- SD card

The i.MX 95 uses four boot signals to select the boot source, but these signals are not dedicated to this function. The levels of these signals are read in analogy to previous i.MX CPUs when the reset is disabled, and must be set high or low depending on the desired boot source at read-in time.

Table 5: Boot signals

Signal (multiplexing)	CPU-Pin	Power-Group
UART1_TXD (BOOT_MODE0)	[F52] UART1_TXD	NVCC_AON (3.3 V)
UART2_TXD (BOOT_MODE1)	[F48] UART2_TXD	
SAI1_TXFS (BOOT_MODE2)	[G49] SAI1_TXFS	
SAI1_TXD0 (BOOT_MODE3)	[H48] SAI1_TXD0	

The exact boot source configuration is shown in the following figure. The i.MX 95 only supports Low Power Boot (LPB - i.e. start of the M33 core), so BOOT_MODE3 must always be set to high. The A55 cores are started by the M33, which acts as the system controller.

Table 6: Boot source selection

BOOT_MODE [3:0]	Functions
0101	Reserved
0110	Reserved
0111	Reserved
1000	Boot from Internal Fuses
1001	Serial Downloader (USB1)
1010	uSDHC1, 8-bit, 1.8 V, eMMC 5.1
1011	uSDHC2, 4-bit, SD 3.0
1100	FlexSPI Serial NOR
1101	FlexSPI Serial NAND 2K
1110	FlexSPI Serial NAND 4K
1111	Reserved

More information about boot interfaces and its configuration is to be taken from the i.MX 95 Data Sheet (1) and the i.MX 95 Reference Manual (2). Alternatively, an image can be loaded into the internal RAM via serial downloader.

Note: Field software updates	
	When designing a carrier board, it is recommended to have a redundant update concept for field software updates.

3.5 Memory

3.5.1 RAM

LPDDR5-RAM with a memory width of 32 bits is used on the TQMa95xxLA. The i.MX 95 supports Inline ECC.
The LPDDR memory interface has the following basic parameters:

Table 7: Parameter RAM interface

Parameter	i.MX 95
Memory type	LPDDR4X / LPDDR5
DDR timing	max. LPDDR5-6400
DDR clock frequenz	max. 3200 MHz
Bus width (data)	32 bit
Max. memory size	16 GByte

The standard memory size of the TQMa95xxLA is 2 GByte. Variants with 4 GByte and 8 GByte are available.

Attention: Malfunction	
	The TQMa95xxLA uses a specially developed RAM timing. Each memory expansion level required its own RAM configuration.

3.5.2 eMMC

An eMMC is available on the TQMa95xxLA as non-volatile memory for programs and data (e.g. bootloader, operating system, application). The following figure shows the interface of the eMMC to the i.MX 95:

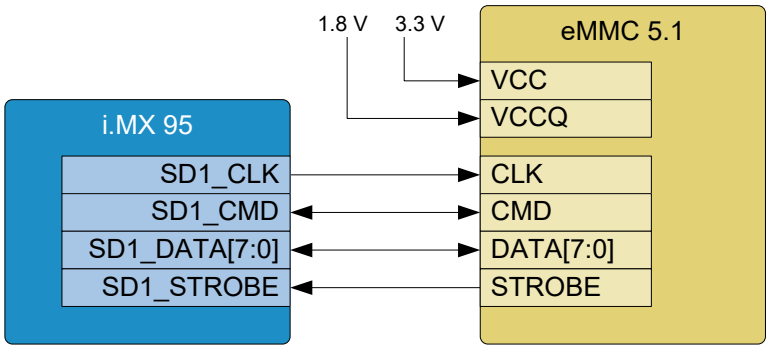

Figure 4: Block diagram eMMC

The eMMC is connected via the USDHC1 interface of the i.MX 95. A maximum transfer rate of 400 MB/s is supported, which corresponds to HS400 mode. Series resistors are provided for the CLK, DATA and CMD signals.
The standard eMMC is SanDisks SDINBDG4-8G-XI2 (8 GByte / MLC).

Table 8: Pin assignment eMMC via SD1

Signal (multiplexing)	CPU-Pin	Power-Group
SD1_CLK	[AG39] SD1_CLK	NVCC_WAKEUP (1.8 V)
SD1_CMD	[AF40] SD1_CMD	
SD1_DATA0	[AG45] SD1_DATA0	
SD1_DATA1	[AE45] SD1_DATA1	
SD1_DATA2	[AD46] SD1_DATA2	
SD1_DATA3	[AG43] SD1_DATA3	
SD1_DATA4	[AF44] SD1_DATA4	
SD1_DATA5	[AG47] SD1_DATA5	
SD1_DATA6	[AD44] SD1_DATA6	
SD1_DATA7	[AC45] SD1_DATA7	
SD1_STROBE	[AG41] SD1_STROBE	

3.5.3 NOR Flash

With XSPI, the CPU provides an 8-bit wide, bootable interface that can be used to connect an optional module-internal flash. QSPI NOR Flash is used here, which results in a restriction of the XSPI interface outside the TQMa95xxLA. For this reason, 33 Ω series resistors are provided in the DATA[3:0] signals. The other signals DATA[7:4] are implemented without external wiring. If the NOR flash is not installed, all signals of the XSPI interface can be used outside the module. The supply voltage of the flash is 1.8 V. If no NOR Flash is installed the series resistors are populated with 0 Ω.

The standard NOR flash is Winbond W25Q512NWBIQ (64 MByte).

3.5.4 EEPROM

The TQMa95xxLA is available with an optional EEPROM that is connected via I2C. This contains a separate memory area - the "Identification Page" - which can be write-protected if required and is therefore used to store sensitive data. The memory size can also be customized by changing the EEPROM configuration.

The following table shows details of the default EEPROM:

Table 9: EEPROM

Manufacturer	Part number	Size	Temperature range
ST Microelectronics	M24C64-DFMC6TG	64 Kbit	–40 °C to +85 °C

3.5.5 SD Card

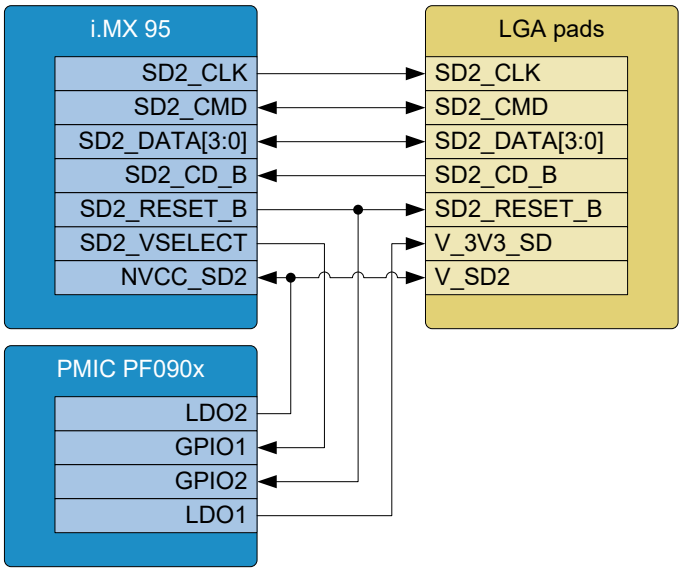

Figure 5: Block diagram SD Card

The i.MX 95 supports SD cards up to UHS-I in SDR104/DDR50 mode. This corresponds to the SD card specification v3.0 and a maximum data width of 4 bits.

To allow booting from SD cards, the SD2 interface is routed to the outside with the exception of SD2_VSELECT. SD2_RESET_B is routed to the outside, but can remain unconnected, since the actual reset function of this signal is already implemented on the module.

The SD2 interface signals are supplied by a separate PMIC LDO whose IO voltage can be set to a range of 1.8 V or 3.3 V using the SD2_VSELECT signal. SD2_VSELECT is automatically toggled by the driver to use the fastest possible mode depending on the SD card used.

Due to an internal module pull-down on SD2_VSELECT, the default setting at boot time is 3.3 V.

Table 10: LDO voltage control via SD2_VSELECT

Level SD2_VSELECT	PMIC voltage V_SD2
Low	typ. 3.3 V
High	typ. 1.8 V

The supply voltage V_SD2 is also provided externally by the module. In customer designs, this voltage can be used to connect the pull-up resistors of the SD card interface. Alternatively, the internal pull-up resistors of the CPU can be used.
The voltage V_3V3_SD is used to supply the SD card. The module-internal wiring allows to interrupt the SD card supply in case of a module reset, thus allowing a reset of the SD card.

Table 11: Pin assignment SD2 (SD Card)

Signal (multiplexing)	CPU pin	Power group
SD2_CD#	[AD48] SD2_CD_B	NVCC_SD2 (1.8 V / 3.3 V)
SD2_CLK	[AB48] SD2_CLK	
SD2_CMD	[AB52] SD2_CMD	
SD2_DATA0	[AC51] SD2_DATA0	
SD2_DATA1	[AC49] SD2_DATA1	
SD2_DATA2	[AA51] SD2_DATA2	
SD2_DATA3	[AA49] SD2_DATA3	
SD2_RST#	[AD52] SD2_RESEST_B	

3.5.6 USDHC3

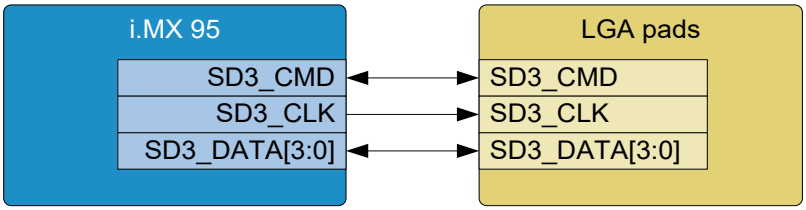

Figure 6: Block diagram USDHC3

In addition to SD2, the CPU has an additional four-bit SDIO interface that cannot be used as a boot source. This interface can still be used, for example, to connect M.2 slots or similar. All corresponding signals are provided at LGA pads without further wiring. If no SDIO interface is needed, these pins can be used as GPIOs.

Table 12: USDHC3

Signal (multiplexing)	CPU pin	Power group
SD3_DATA0	[AG49] SD3_DATA0	NVCC_WAKEUP (1.8 V)
SD3_DATA1	[AH52] SD3_DATA1	
SD3_DATA2	[AE49] SD3_DATA2	
SD3_DATA3	[AF52] SD3_DATA3	
SD3_CMD	[AF48] SD3_CMD	
SD3_CLK	[AG51] SD3_CLK	

3.6 Temperature sensor

The NXP SE97BTP temperature sensor with integrated EEPROM is used for temperature measurement. The TEMP_EVENT# alarm output is routed to the outside and can be flexibly connected as an open-drain output. The sensor is controlled by the I2C1 bus (address: 0x1B).

The integrated EEPROM serves as a manufacturer's EEPROM for TQ and is not intended for use by customers.

3.7 i.MX 95 internal RTC

The i.MX 95 has an internal RTC. Its accuracy is primarily determined by the characteristics of the quartz used. The type FC-135 used on the TQMa95xxLA has a standard frequency tolerance of ±20 ppm at +25 °C. (Parabolic coefficient: max. -0.04 x 10^{-6} / °C^2)

3.8 Optional RTC PCF85063

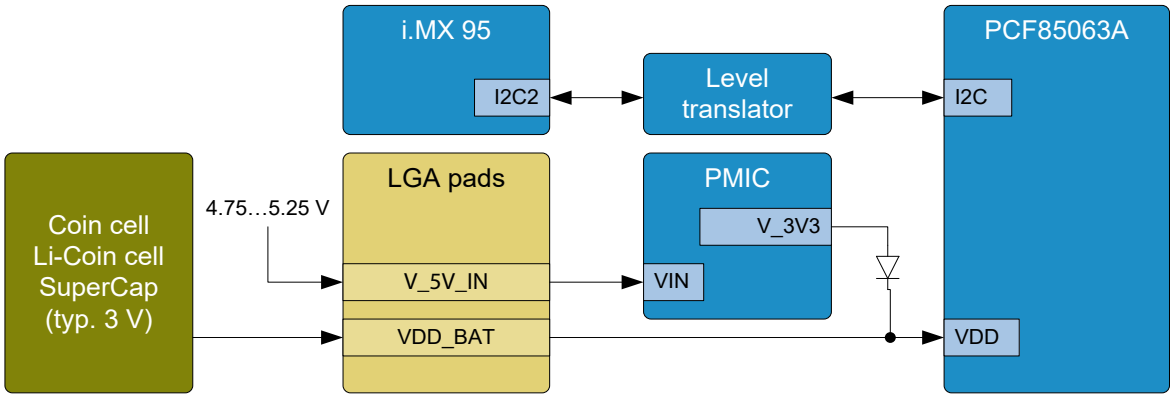

Figure 7: Block diagram RTC supply (TQMa95xxLA with discrete RTC)

In addition to the i.MX 95 internal RTC, TQMa95xxLA variants with discrete RTC at I2C2 are available. It is recommended to use the RTC PCF85063 due to the lower current consumption during standby modes. The RTC_INT# signal is routed to the LGA pad and can be used as an open-drain signal in customer designs.

- The discrete RTC has I2C2 address `0x51 / 101 0001b`

3.9 Gyroscope

An optional gyroscope with I2C and SPI interfaces is provided on the TQMa95xxLA. It allows to determine the position of the TQMa95xxLA and provides two interrupts. These are routed to the outside and are available at two LGA pads. It is connected via I2C2 (address: `0x6B / 110 1011b`).

3.10 1G Ethernet (RGMII)

The i.MX 95 has two Ethernet MACs, each operating in maximum Gigabit full-duplex mode. MII, RMII, or RGMII can be used as the preferred interface, with the latter being used for standard muxing. On the muxing side, only one common MDIO/SMI interface is available for both MACs.

ENET1 supports both QOS (Quality of Service) and TSN (Time-sensitive Network).

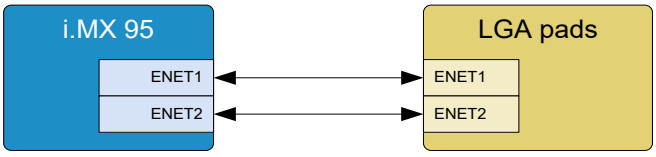

Figure 8: Block diagram 1G Ethernet (RGMII)

An IO voltage of 1.8 V is specified for RGMII and an IO voltage of either 1.8 V or 3.3 V is specified for RMII. Since both modes operate at 1.8 V, the NVCC_ENET rail is set to 1.8 V.

The following table shows the ENET interface signals:

Table 13: Pin assignment RGMII

Signal (multiplexing)	CPU pin	Power group
ENET1_RX_CTL	[AH34] ENET1_RX_CTL	NVCC_ENET (1.8 V)
ENET1_RXC	[AJ33] ENET1_RXC	
ENET1_RD0	[AJ35] ENET1_RD0	
ENET1_RD1	[AK36] ENET1_RD1	
ENET1_RD2	[AJ37] ENET1_RD2	
ENET1_RD3	[AH38] ENET1_RD3	
ENET1_TX_CTL	[AF32] ENET1_TX_CTL	
ENET1_TXC	[AG31] ENET1_TXC	
ENET1_TD0	[AG33] ENET1_TD0	
ENET1_TD1	[AG35] ENET1_TD1	
ENET1_TD2	[AF36] ENET1_TD2	
ENET1_TD3	[AG37] ENET1_TD3	
ENET1_MDC	[AK40] ENET1_MDC	
ENET1_MDIO	[AJ39] ENET1_MDIO	
ENET2_RX_CTL	[AH26] ENET2_RX_CTL	
ENET2_RXC	[AJ25] ENET2_RXC	
ENET2_RD0	[AJ27] ENET2_RD0	
ENET2_RD1	[AK28] ENET2_RD1	
ENET2_RD2	[AJ29] ENET2_RD2	
ENET2_RD3	[AH30] ENET2_RD3	
ENET2_TX_CTL	[AF24] ENET2_TX_CTL	
ENET2_TXC	[AG23] ENET2_TXC	
ENET2_TD0	[AG25] ENET2_TD0	
ENET2_TD1	[AG27] ENET2_TD1	
ENET2_TD2	[AF28] ENET2_TD2	
ENET2_TD3	[AG29] ENET2_TD3	
ENET2_MDC	[AK32] ENET2_MDC	
ENET2_MDIO	[AJ31] ENET2_MDIO	

3.11 10G Ethernet (XGMII)

In addition to the two 1G Ethernet interfaces, some i.MX 95 derivatives also have a 10G Ethernet interface. This interface is provided at module pins without any additional wiring.

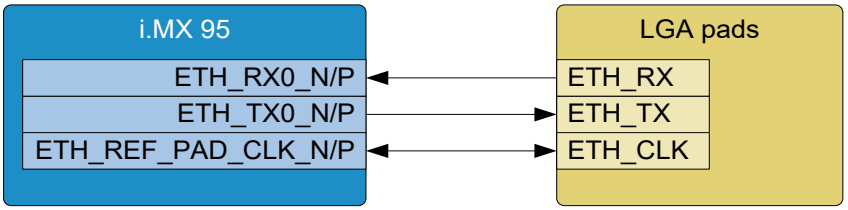

Figure 9: Block diagram 10G Ethernet (XGMII)

Table 14: Pin assignment XGMII

Signal (multiplexing)	CPU pin	Power group
ETH_RX_N	[AK12] ETH_RX0_N	VDD_ETH_0P8 (0.8 V)
ETH_RX_P	[AJ13] ETH_RX0_P	
ETH_REF_CLK_N	[AF14] ETH_REF_PAD_CLK_N	
ETH_REF_CLK_P	[AG15] ETH_REF_PAD_CLK_P	
ETH_TX_N	[AK16] ETH_TX0_N	
ETH_TX_P	[AJ17] ETH_TX0_P	

3.12 USB

The i.MX 95 has a USB 2.0 controller (USB2) and a USB 3.0 controller (USB1). Both can be configured as host or device. The superspeed signals of the USB 3.0 controller can be connected directly to a USB-C connector as the controller provides two differential Tx and Rx pairs.

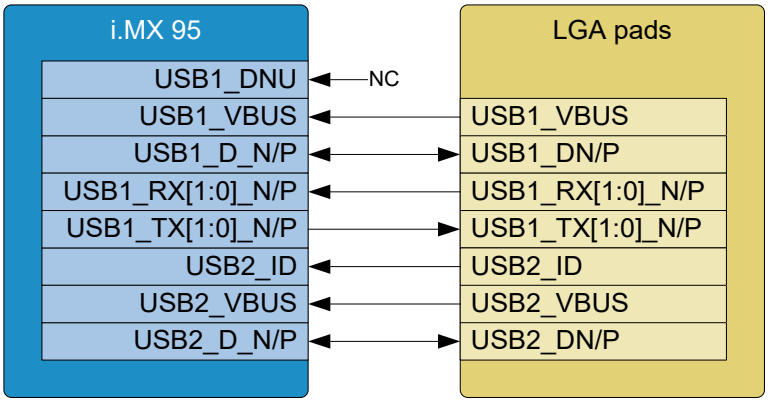

Figure 10: Block diagram USB

The USB1_ID signal has no function and is left unconnected. USB2_ID is correctly implemented and can be used to detect the host or device role. The OTG_OC (Over-Current) and OTG_PWR signals are not available by default on either controller, as their multiplexing overlaps with the ENET1 interfaces.

The VBUS signals both have 30 kΩ series resistors on the module. According to NXP's i.MX 95 Hardware Developer's Guide, it is therefore possible to apply external 5V to these pins. The USB*_TXRTUNE pins are connected to GND with 200 Ohm resistors. The differential USB signals must have a differential impedance of 90 Ω.

USB1 also serves as a serial download port during boot.

Table 15: Pin assignment USB

Signal (multiplexing)	CPU pin	Power group
NC	[C23] USB1_DNU	Internal 1.8 V
USB2_ID	[F24] USB2_ID	VDD_USB_1P8 (1.8 V)
-	[F28] USB2_TXRTUNE	
USB1_DN USB1_DP	[B18] USB1_D_N [C19] USB1_D_P	VDD_USB_3P3 (3.3 V)
USB1_VBUS	[E23] USB1_VBUS	
-	[B22] USB1_TXRTUNE	
USB2_DN USB2_DP	[A25] USB2_D_N [B24] USB2_D_P	
USB2_VBUS	[E27] USB2_VBUS	
USB1_RX0_N USB1_RX0_P	[B20] USB1_RX0_N [A21] USB1_RX0_P	VDD_USB_0P8 (0.8 V)
USB1_RX1_N USB1_RX1_P	[A17] USB1_RX1_N [B16] USB1_RX1_P	
USB1_TX0_N USB1_TX0_P	[E25] USB1_TX0_N [D26] USB1_TX0_P	
USB1_TX1_N USB1_TX1_P	[D22] USB1_TX1_N [E21] USB1_TX1_P	

3.13 LVDS

The i.MX 95 has two LVDS controllers with four differential data pairs for data transfer. The LVDS PHYs support outputs up to 1080p at 60 fps.

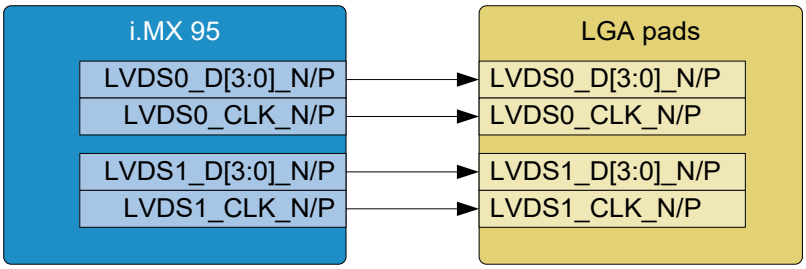

Figure 11: Block diagram LVDS

The differential signals have an differential impedance of 100 Ω. The interfaces are routed directly to the outside of the module without any internal wiring.

Table 16: Pin assignment LVDS

Signal (multiplexing)	CPU pin	Power group
LVDS0_D0_N LVDS0_D0_P	[G9] LVDS0_D0_N [G7] LVDS0_D0_P	VDD_LVDS_1P8 (1.8 V)
LVDS0_D1_N LVDS0_D1_P	[F8] LVDS0_D1_N [F6] LVDS0_D1_P	
LVDS0_D2_N LVDS0_D2_P	[E7] LVDS0_D2_N [D6] LVDS0_D2_P	
LVDS0_D3_N LVDS0_D3_P	[E9] LVDS0_D3_N [D8] LVDS0_D3_P	
LVDS0_CLK_N LVDS0_CLK_P	[A5] LVDS0_CLK_N [B4] LVDS0_CLK_P	
LVDS1_D0_N LVDS1_D0_P	[A3] LVDS1_D0_N [B2] LVDS1_D0_P	
LVDS1_D1_N LVDS1_D1_P	[C3] LVDS1_D1_N [C1] LVDS1_D1_P	
LVDS1_D2_N LVDS1_D2_P	[E3] LVDS1_D2_N [E1] LVDS1_D2_P	
LVDS1_D3_N LVDS1_D3_P	[F4] LVDS1_D3_N [F2] LVDS1_D3_P	
LVDS1_CLK_N LVDS1_CLK_P	[D4] LVDS1_CLK_N [D2] LVDS1_CLK_P	

3.14 MIPI CSI

The i.MX 95 provides up to two MIPI-CSI interfaces. These are camera inputs with four differential data pairs. They can transfer up to 2.5 Gbps per data pair. The image resolution is up to 4K at 30 fps.

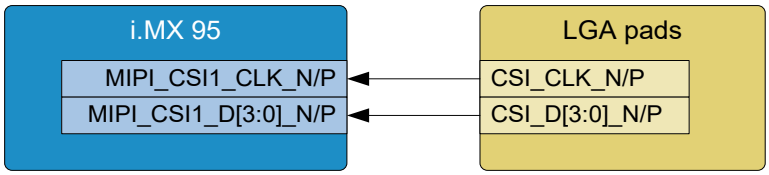

Figure 12: Block diagram CSI

CSI1 is a dedicated interface. The second CSI interface can alternatively be multiplexed as MIPI DSI.
The differential signals have a differential impedance of 100 Ω. The interface is routed directly to the outside without any further internal module wiring.

Table 17: Pin assignment MIPI CSI

Signal (multiplexing)	CPU pin	Power group
MIPI_CSI1_D0_N MIPI_CSI1_D0_P	[F20] MIPI_CSI1_D0_N [E19] MIPI_CSI1_D0_P	VDD_MIPI_1P8 (1.8 V)
MIPI_CSI1_D1_N MIPI_CSI1_D1_P	[D18] MIPI_CSI1_D1_N [E17] MIPI_CSI1_D1_P	
MIPI_CSI1_D2_N MIPI_CSI1_D2_P	[D14] MIPI_CSI1_D2_N [E13] MIPI_CSI1_D2_P	
MIPI_CSI1_D3_N MIPI_CSI1_D3_P	[F12] MIPI_CSI1_D3_N [E11] MIPI_CSI1_D3_P	
MIPI_CSI1_CLK_N MIPI_CSI1_CLK_P	[F16] MIPI_CSI1_CLK_N [F15] MIPI_CSI1_CLK_P	

3.15 MIPI DSI / CSI

The second MIPI interface of the i.MX 95 is a combined MIPI-CSI / DSI interface, i.e. data output or data input is possible. This interface also has four differential data pairs that can transfer up to 2.5 Gbps. A resolution of up to 4K at 30 fps is also possible.

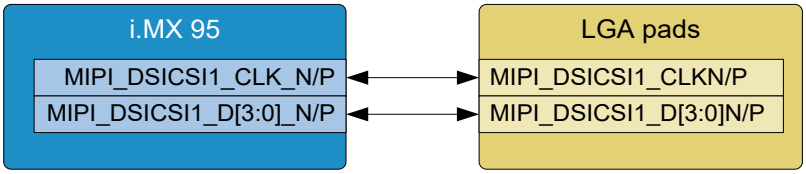

Figure 13: Block diagram CSI / DSI

The differential signals have a differential impedance of 100 Ω. The interface is routed directly to the outside without any further internal module circuitry.

Table 18: Pin assignment DSI / CSI

Signal (multiplexing)	CPU pin	Power group
MIPI_DSICSI1_D0_N MIPI_DSICSI1_D0_P	[C15] MIPI_DSICSI1_D0_N [B14] MIPI_DSICSI1_D0_P	VDD_MIPI_1P8 (1.8 V)
MIPI_DSICSI1_D1_N MIPI_DSICSI1_D1_P	[A13] MIPI_DSICSI1_D1_N [B12] MIPI_DSICSI1_D1_P	
MIPI_DSICSI1_D2_N MIPI_DSICSI1_D2_P	[A9] MIPI_DSICSI1_D2_N [B8] MIPI_DSICSI1_D2_P	
MIPI_DSICSI1_D3_N MIPI_DSICSI1_D3_P	[C7] MIPI_DSICSI1_D3_N [B6] MIPI_DSICSI1_D3_P	
MIPI_DSICSI1_CLK_N MIPI_DSICSI1_CLK_P	[C11] MIPI_DSICSI1_CLK_N [B10] MIPI_DSICSI1_CLK_P	

3.16 Tamper

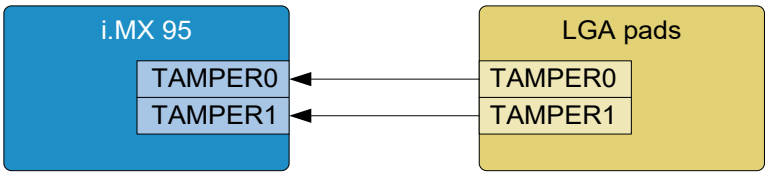

Figure 14: Block diagram Tamper

A total of two tamper signals are provided as one of the security features of the i.MX 95's BBSM unit. These are routed to LGA pads without any additional wiring.

Table 19: Pin assignment Tamper

Signal (multiplexing)	CPU pin	Power group
TAMPER0	[F36] TAMPER0	NVCC_BBSM (1.8 V)
TAMPER1	[D38] TAMPER1	

3.17 SAI

The i.MX 95 has several SAI interfaces with different data bus widths. Due to limited multiplexing capabilities, none of these interfaces are used natively. Instead, the outgoing SAI1 signals are used as CAN or GPIO, for example.

All SAI interfaces support I2S, AC97, TDM and other codec interfaces.

Table 20: Pin assignment SAI

Signal (multiplexing)	CPU pin	Power group
SAI1_TXC	[G51] SAI1_TXC	NVCC_AON (3.3 V)
SAI1_TXFS	[G49] SAI1_TXFS	
SAI1_TXD0	[H48] SAI1_TXD0	
SAI1_RXD0	[H52] SAI1_RXD0	

3.18 eARC

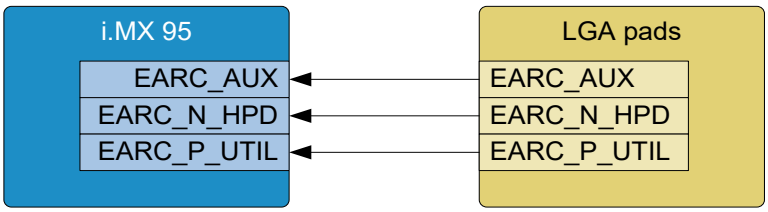

Figure 15: Block diagram eARC

In addition to SAI, the i.MX 95 also features an eARC interface that can be used as an audio input if desired. The corresponding signals are routed to LGA padswithout any additional wiring.

Table 21: Pin assignment eARC

Signal (multiplexing)	CPU pin	Power group
EARC_N_HPD	[Y46] EARC_N_HPD	VDD_EARC_1P8 (1.8 V)
EARC_P_UTIL	[Y44] EARC_P_UTIL	
EARC_AUX	[AA45] EARC_AUX	

3.19 PDM

The CPU provides a PDM interface that can be used as a microphone input. However, as the native CPU pins also allow other functions, the pins are used for other purposes. If a PDM interface is required, it should be taken from the GPIO2 domain, as this offers more lanes for a more extensive interface. For example, the CPU pin PDM_CLK is used to connect the PMIC_INT# signal and is not routed to the outside. PDM_BIT_STREAM1 allows muxing as M33_NMI.

Table 22: Pin assignment PDM

Signal (multiplexing)	CPU pin	Power group
PDM_BIT0	[G45] PDM_BIT_STREAM0	NVCC_AON (3.3 V)
PDM_BIT1	[H46] PDM_BIT_STREAM1	

3.20 Serial ports

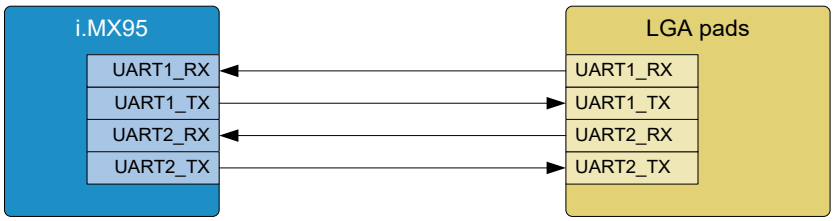

Figure 16: Block diagram UART

The CPU provides up to eight UARTs. Two of them are available by default. Both are in the AON domain and are therefore assigned to the Cortex M33 / system controller.

Table 23: Pin assignment UART

Signal (multiplexing)	CPU pin	Power group
UART1_RX	[E49] UART1_RXD	NVCC_AON (3,3 V)
UART1_TX	[F52] UART1_TXD	
UART2_RX	[E51] UART2_RXD	
UART2_TX	[F48] UART2_TXD	

3.21 PCI Express

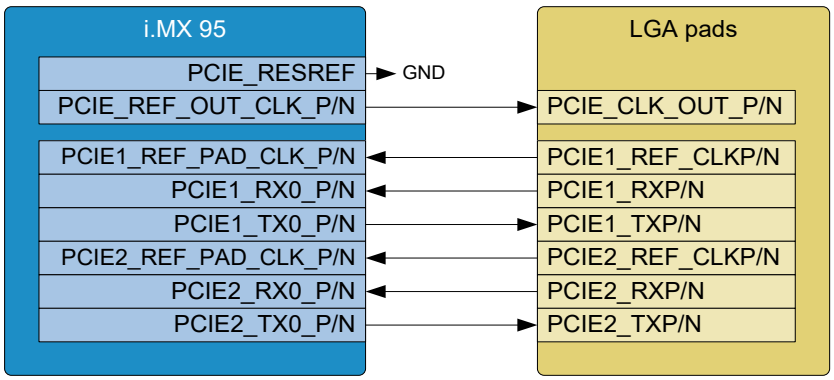

Figure 17: Block diagram PCI Express

The i.MX 95 has two PCIe 3.0 interfaces, each with one lane. A separate clock output is also provided. It is not possible to connect the clock output directly to the clock inputs because the technologies are not compatible (LVDS to HCSL). For this reason, a

buffer or an external clock generator is always required to supply the clock inputs! Corresponding circuitry must always be implemented on the mainboard.

Table 24: Pin assignment PCIe

Signal (multiplexing)	CPU pin	Power group
PCIE1_REF_CLKN	[C31] PCIE1_REF_PAD_CLK_N	VDD_PCI_1P8 (1.8 V)
PCIE1_REF_CLKP	[B30] PCIE1_REF_PAD_CLK_P	
PCIE1_RXN	[A29] PCIE1_RX0_N	
PCIE1_RXP	[B28] PCIE1_RX0_P	
PCIE1_TXN	[D30] PCIE1_TX0_N	
PCIE1_TXP	[E29] PCIE1_TX0_P	
PCIE2_REF_CLKN	[A33] PCIE2_REF_PAD_CLK_N	
PCIE2_REF_CLKP	[B32] PCIE2_REF_PAD_CLK_P	
PCIE2_RXN	[C35] PCIE2_RX0_N	
PCIE2_RXP	[B34] PCIE2_RX0_P	
PCIE2_TXN	[F32] PCIE2_TX0_N	
PCIE2_TXP	[E31] PCIE2_TX0_P	
PCIE_CLK_OUT_N	[C27] PCIE_REF_OUT_CLK_N	VDD_ANAVDET_1P8 (1.8 V)
PCIE_CLK_OUT_P	[B26] PCIE_REF_OUT_CLK_P	

3.22 I²C

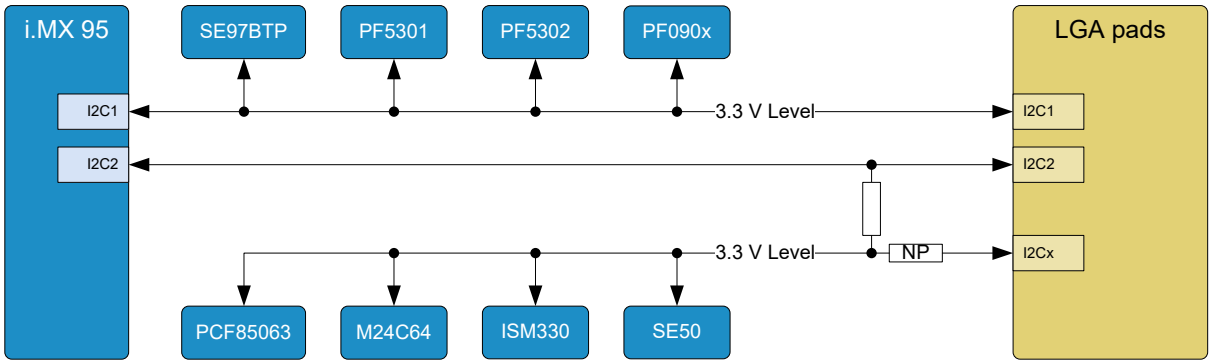

Figure 18: Block diagram I²C

The i.MX 95 provides up to eight I2C interfaces. I2C1 serves as the Cortex-M33 system bus for PMICs and temperature sensor, has pull-ups on the module and is also routed to LGA pads.

The other internal components RTC, EEPROM, TSE and gyroscope are combined in a separate bus, which can be connected either to I2C2 or to another I2C bus. Due to the supply voltages specified on the module for these components, this other bus must have a 3.3V level as well.

Other buses can be provided on the GPIO2 pins without wiring on the module. Their voltage level is defined by V_GPIO. In this case, pull-up resistors must be placed outside the module.

The internal components of the TQMa95xxLA with their corresponding addresses are listed in the following table:

Table 25: I²C addresses

Bus	I2C -Slave	Address	Remark
I2C1	Temperature Sensor SE97BTP	0x1B	Temperature Sensor
		0x53	EEPROM Read/Write
		0x33	EEPROM Protection Command
	PMIC PF090x	0x08	-
	PMIC PF5301	0x2A	-
	PMIC PF5302	0x29	-
I2C2	RTC PCF85063ATL	0x51	-
	Secure Element SE050	0x48	-
	Gyroskop ISM330	0x6B	-
	EEPROM M24C64	0x54	Memory Array
		0x5C	Identification Page (32 Bytes)

A list of the available I2C buses can be found in the following table:

Table 26: Pin assignment I2C

Signal (multiplexing)	CPU pin	Power group
I2C1_SCL	[D48] I2C1_SCL	NVCC_AON (3,3 V)
I2C1_SDA	[D52] I2C1_SDA	
I2C2_SCL	[E43] I2C2_SCL	
I2C2_SDA	[E45] I2C2_SDA	
I2Cx	other	NVCC_ GPIO (1,8 V / 3,3 V)

3.23 GPIO

With the exception of dedicated differential signals (e.g. MIPI DSI/CSI, LVDS), most of the CPU pins can be configured as GPIOs. GPIO1_IO08 is not routed to the outside and is used internally to connect the open-drain signal PMIC_INT#. As a freely configurable group, the signals of the NVCC_GPIO power domain can be used not only as GPIOs, but also as I2C, SPI or SAI interfaces, for example.

Table 27: Pin assignment GPIO

Signal (multiplexing)	CPU pin	Power group
GPIO2_IO00	[J49] GPIO_IO00	NVCC_ GPIO (1.8 V / 3.3 V)
GPIO2_IO01	[J51] GPIO_IO01	
GPIO2_IO02	[K48] GPIO_IO02	
GPIO2_IO03	[K52] GPIO_IO03	
GPIO2_IO04	[K46] GPIO_IO04	
GPIO2_IO05	[L45] GPIO_IO05	
GPIO2_IO06	[L49] GPIO_IO06	
GPIO2_IO07	[L51] GPIO_IO07	
GPIO2_IO08	[M44] GPIO_IO08	
GPIO2_IO09	[M46] GPIO_IO09	
GPIO2_IO10	[M48] GPIO_IO10	
GPIO2_IO11	[M52] GPIO_IO11	
GPIO2_IO12	[N45] GPIO_IO12	
GPIO2_IO13	[N49] GPIO_IO13	
GPIO2_IO14	[N51] GPIO_IO14	
GPIO2_IO15	[P44] GPIO_IO15	
GPIO2_IO16	[P46] GPIO_IO16	
GPIO2_IO17	[P48] GPIO_IO17	
GPIO2_IO18	[P52] GPIO_IO18	
GPIO2_IO19	[R45] GPIO_IO19	
GPIO2_IO20	[R49] GPIO_IO20	
GPIO2_IO21	[R51] GPIO_IO21	
GPIO2_IO22	[T44] GPIO_IO22	
GPIO2_IO23	[T46] GPIO_IO23	
GPIO2_IO24	[T48] GPIO_IO24	
GPIO2_IO25	[T52] GPIO_IO25	
GPIO2_IO26	[U45] GPIO_IO26	
GPIO2_IO27	[U49] GPIO_IO27	
GPIO2_IO28	[U51] GPIO_IO28	
GPIO2_IO29	[V44] GPIO_IO29	
GPIO2_IO30	[V46] GPIO_IO30	
GPIO2_IO31	[V48] GPIO_IO31	
GPIO5_IO12	[V52] GPIO_IO32	
GPIO5_IO13	[W45] GPIO_IO33	
GPIO5_IO14	[W49] GPIO_IO34	
GPIO5_IO15	[W51] GPIO_IO35	
GPIO5_IO16	[Y48] GPIO_IO36	
GPIO5_IO17	[Y52] GPIO_IO37	

3.24 Watchdog

The watchdog signal WDOG_ANY of the i.MX 95 is connected to the watchdog input of the PMIC and to the LGA pad.

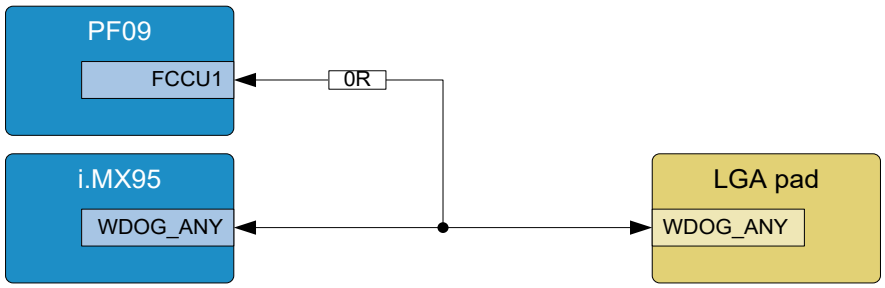

Figure 19: Block diagram Watchdog

3.25 ADC

Figure 20: Block diagram ADC

The i.MX 95 has a 12-bit analog-to-digital converter with a reference voltage of 1.8 V and a maximum of 8 channels. It is not possible to supply an external reference voltage.

Table 28: Pin assignment ADC

Signal (multiplexing)	CPU pin	Power group
ADC_IN0	[A37] ADC_IN0	VDD_ANA_1P8 (1.8 V)
ADC_IN1	[B38] ADC_IN1	
ADC_IN2	[C39] ADC_IN2	
ADC_IN3	[B40] ADC_IN3	
ADC_IN4	[A41] ADC_IN4	
ADC_IN5	[B42] ADC_IN5	
ADC_IN6	[B44] ADC_IN6	
ADC_IN7	[A45] ADC_IN7	

3.26 JTAG

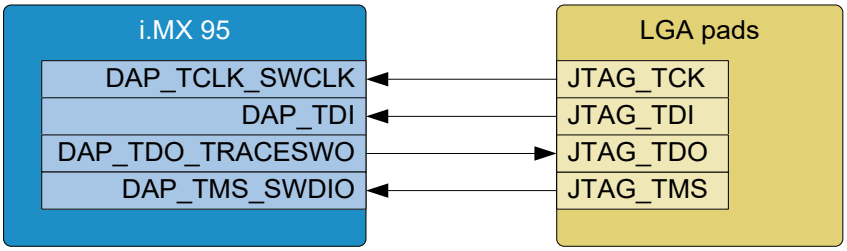

Figure 21: Block diagram JTAG

The JTAG signals are routed directly to LGA pads. Resistors for the pull circuits must be provided on the mainboard.

Table 29: Pin assignment JTAG

Signal (multiplexing)	CPU pin	Power group
JTAG_TCK	[AG21] DAP_TCLK_SWCLK	NVCC_CCM_DAP (1.8 V)
JTAG_TMS	[AH22] DAP_TMS_SWDIO	
JTAG_TDI	[AK24] DAP_TDI	
JTAG_TDO	[AJ23] DAP_TDO_TRACESWO	

3.27 Trust Secure Element

Depending on the module variant, a Trust Secure Element (TSE) is available on the TQMa95xxLA. This is connected to the I2C2 bus (address: `0x48`). The selected chip SE050 from NXP provides additional smartcard interfaces according to ISO14443 and ISO7816 besides the I2C interface. The connection of the antenna for ISO 14443 or the sensor for ISO 7816 must be made on the base board.

If the SE050 is equipped as an option, but no ISO14443 and ISO7816 devices are to be operated, the signals on the motherboard are to be wired as follows:

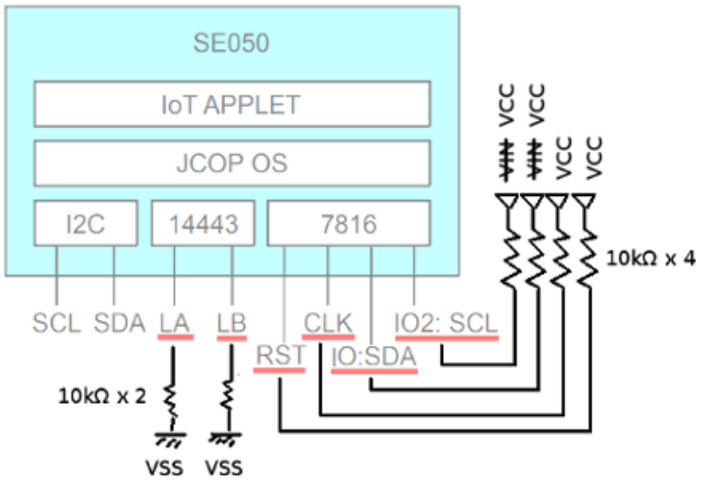

Figure 22: Connecting the NC-Pins
(Source: NXP)

3.28 Power

The TQMa95xxLA is designed for a voltage range of 4.75 V to 5.25 V. All supply voltages required by the CPU and the module components are generated by the TQMa95xxLA. To ensure the correct voltage sequence when powering the module, the individual controllers are enabled in a controlled manner by the PF090x PMIC, which is controlled by a supervisor.

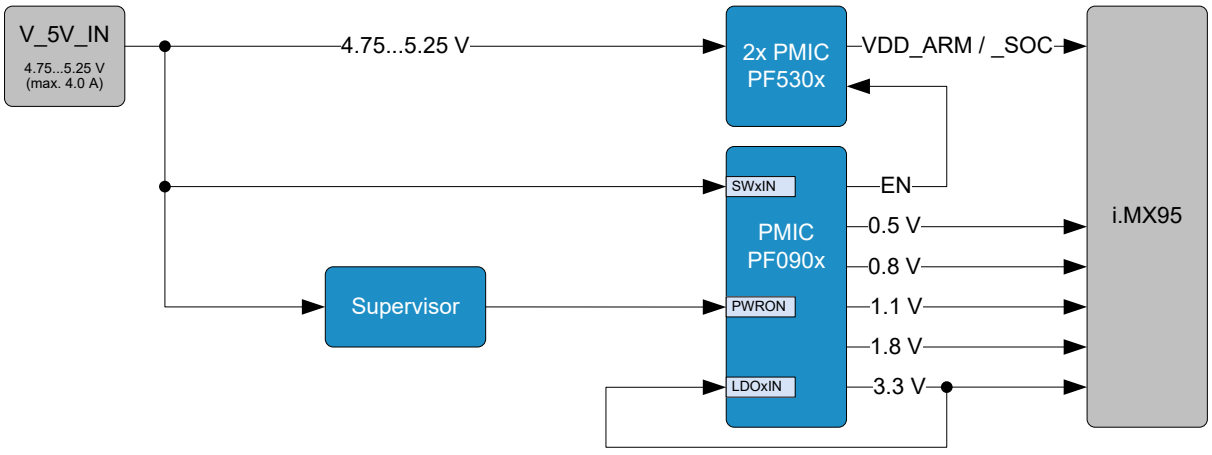

Figure 23: Block diagram module supply

3.28.1 Voltage monitoring

The supervisor of TQMa95xxLA monitors the input voltage and triggers a module reset via the PMIC_ON_REQ signal if the input voltage drops below 4.38 V.

Any protective measures beyond the component's internal protective mechanisms (e.g., overcurrent or reverse polarity protection) must be provided outside the module.

Attention: Malfunction or destruction	
	The voltage monitoring does not detect an exceedance of the maximum permitted input voltage. An excessively high supply voltage can lead to malfunctions, untimely aging or destruction of the TQMa95xxLA.

3.28.2 Power-up sequence TQMa95xxLA

The TQMa95xxLA can be operated with a supply voltage of 4.75 V to 5.25 V and all voltages for normal operation are generated on the module itself.

Attention: Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins should be driven by external components until the power-up sequence has been completed. The mainboard voltages are to be released by V_3V3.

3.28.3 PMIC

Three PMICs are responsible for powering the i.MX 95. The PF090x is the primary PMIC that controls and monitors the other two chips and communicates with them via I2C as needed. The PF5301 and PF5302 PMICs are functionally buck regulators that provide two essential CPU voltages with low voltage but high current. The only difference is their maximum current.

The PF090x has a fixed pre-programmed power sequence in which the two PF530x are integrated. Their enable and PGOOD monitoring is done by the PF090x.

Attention: Malfunction or destruction	
	Improper PMIC programming may cause the i.MX 95 or other peripherals on the TQMa95xxLA to operate outside their specification. This can lead to malfunction, deterioration or destruction of the TQMa95xxLA.

3.29 Reset and Management Signals

Three reset options are provided on the module side:

1. A reset is made possible by the PMIC_ON_REQ signal. This signal between the CPU and PMIC is also routed to the outside, is low-active and has an internal CPU pull-up.
2. A second option is provided by the WDOG_ANY signal. This is a 3.3 V signal which has a pull-up on the module. The associated PMIC behavior can be configured via I2C.
3. RESET_IN# only leads to a partial module reset and should therefore only be used if a reset of the CPU is sufficient. This reset does not reset the memory and peripheral components, among other things.

The ONOFF pin of the CPU offers two reaction options. It has an internal pull-up and is low-active. If this signal is held low for longer than 5 s, the CPU switches to OFF mode. If the signal is briefly pulled low in OFF mode, the CPU switches back to ON mode. A short low pulse in ON mode triggers an interrupt according to (1). In addition, a reset is triggered by a module-internal supervisor when the module supply voltage drops.

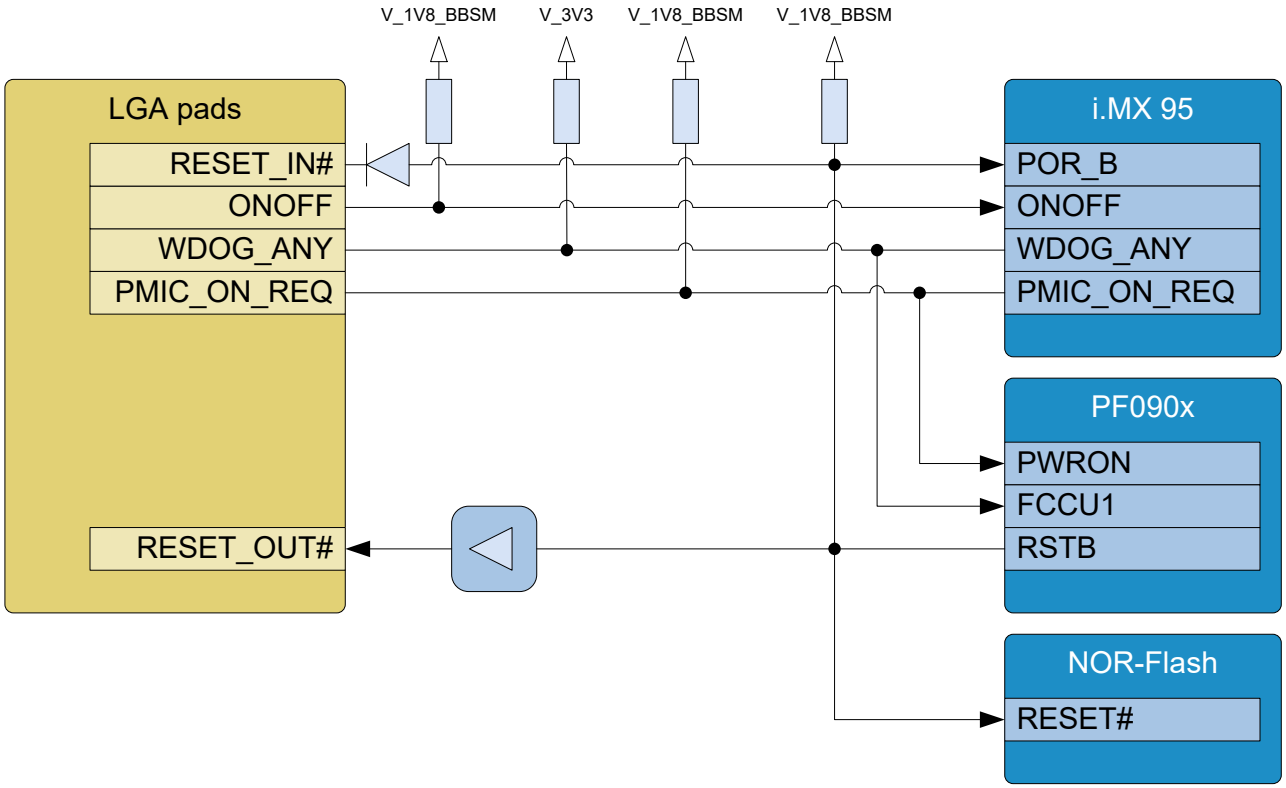

Figure 24: Block diagram Reset

RESET_OUT# is an open-drain output and is routed available at an LGA pad. In customer applications, this ensures feedback to external components when the module is reset. In customer designs, a pull-up is required at this output. The module also has a reset LED.

The FCCU0 signal is used as a fault counter and is only routed internally between the CPU and PMIC. The AMUX, PGOOD and FS0B signals are PMIC status signals, the use of which is up to the user. The function of FS0B differs depending on the application type of the PMIC (QM (Non-Safety Device), Industrial (SIL-2) or Automotive (ASIL-B/C/D)).

The following table lists the reset signals mentioned above, as well as other status signals that cannot be assigned to a more specific group:

Table 30: Reset and management signals

Signal (multiplexing)	CPU pin	Power group
PMIC_STBY_REQ	[C43] PMIC_STBY_REQ	NVCC_BBSM (1.8 V)
PMIC_ON_REQ	[D44] PMIC_ON_REQ	
IMX_ONOFF	[F40] ONOFF	
RESET_IN#	[D42] POR_B	
RESET_OUT#	[D42] POR_B	
PMIC_INT#	[F46] PDM_CLK	NVCC_AON (3.3 V)
FCCU_ERR0	[K44] FCCU_ERR0	
WDOG_ANY	[J45] WDOG_ANY	
AMUX	PMIC PF09 - Pin 15	PMIC internal
PGOOD	PMIC PF09 - Pin 44	Open Drain
FS0B	PMIC PF09 - Pin 54	
RTC_INT#	-	
TEMP_EVENT#	-	
GYRO_INT1	-	
GYRO_INT2	-	

4. MECHANICS

4.1 Dimensions

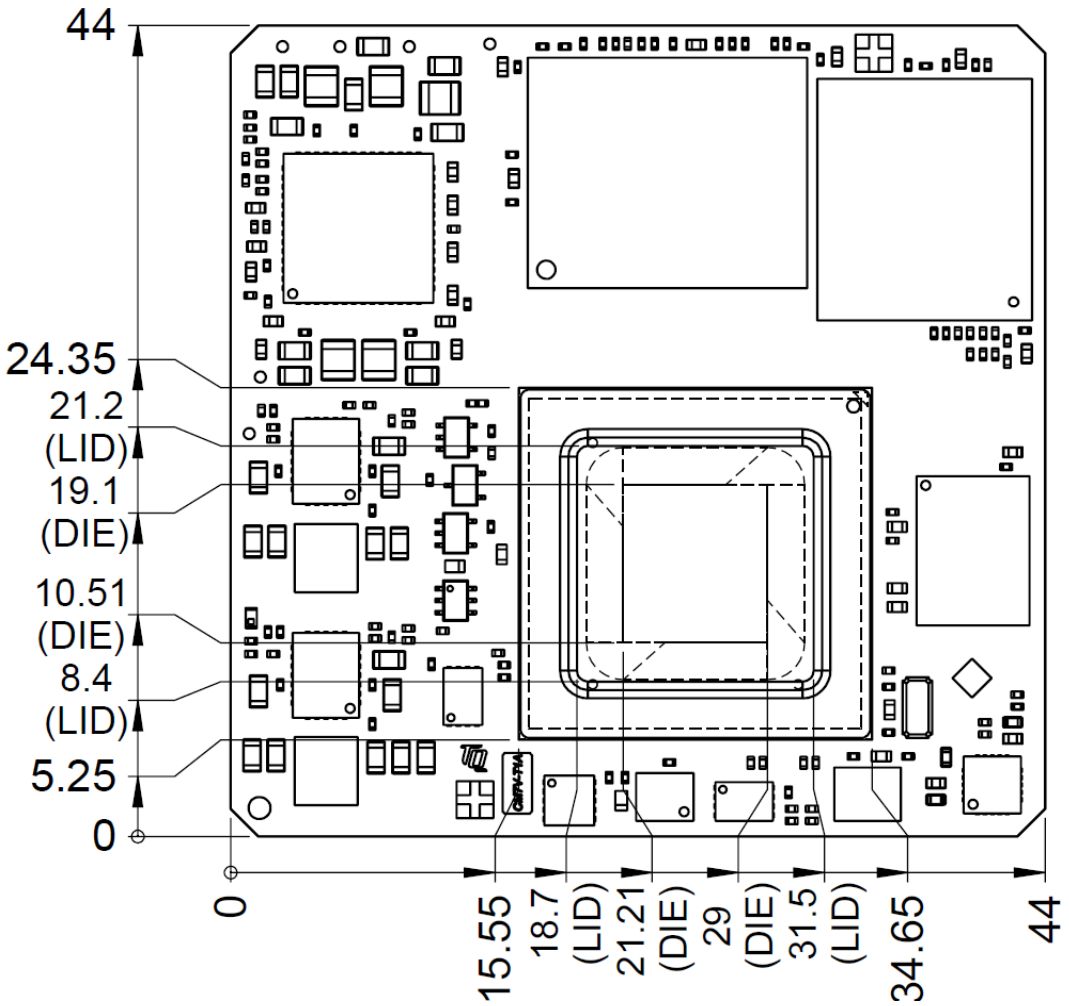

Figure 25: TQMa95xxLA dimensions (top view)

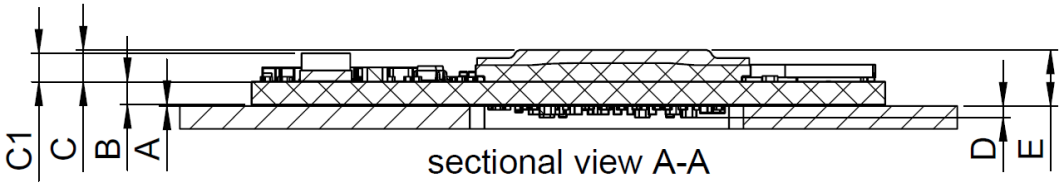

Figure 26: TQMa95xxLA heights with heatspreader

Table 31: Heights

Property	Value	Tolerance	Unit	Comment
A	0.125	+0.075/-0.025	mm	Board to board distance
B	1.50	±0.15	mm	Printed circuit board thickness
C	1.56	±0.18	mm	Processor height (bare die version)
C	2.10	±0.23	mm	Processor height (lidded version)
C1	1.99	±0.08	mm	Inductors
D	0.57	±0.20	mm	Component height below module
E	3.21	±0.24	mm	Overall height to CPU surface (bare die version)
E	3.75	±0.28	mm	Overall height to CPU surface (lidded version)

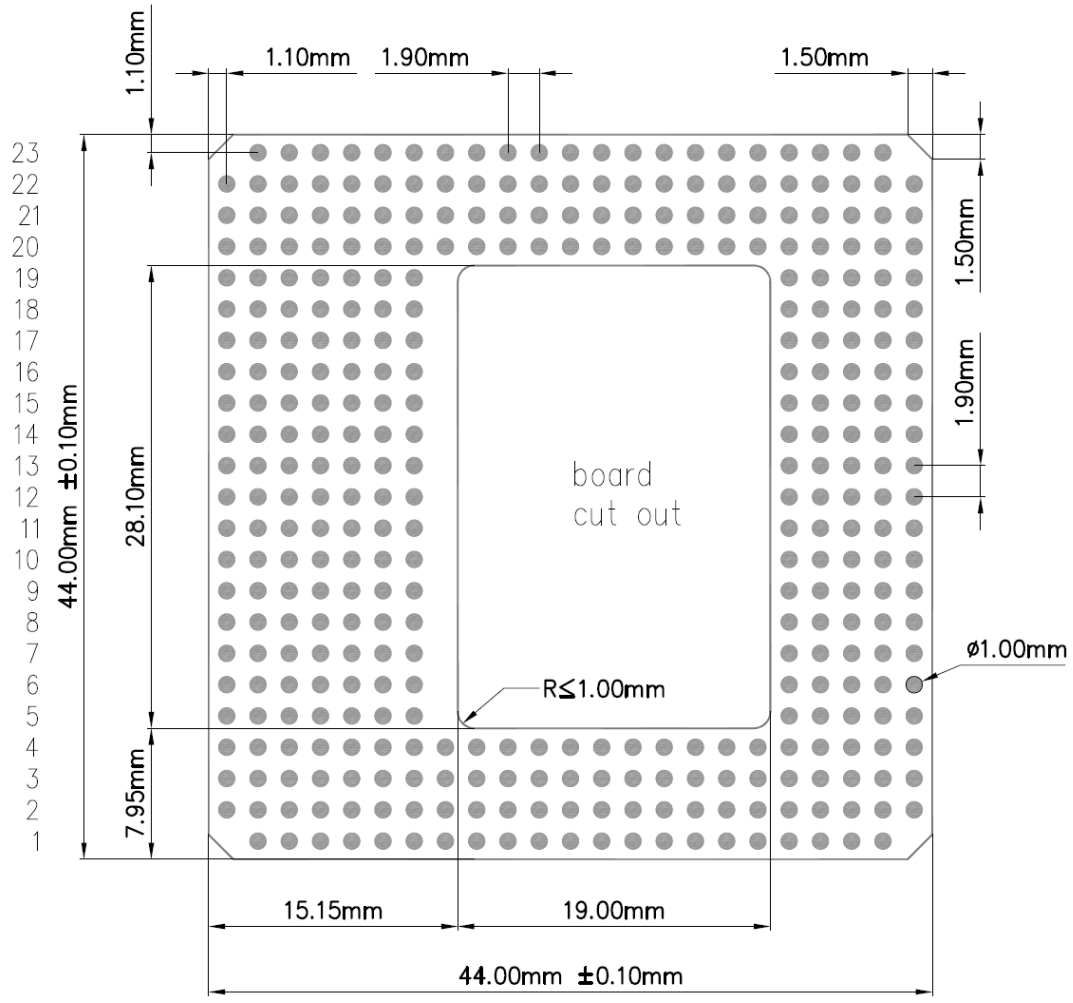

Figure 27: TQMa95xxLA dimensions (bottom view)

4.2 Component placement

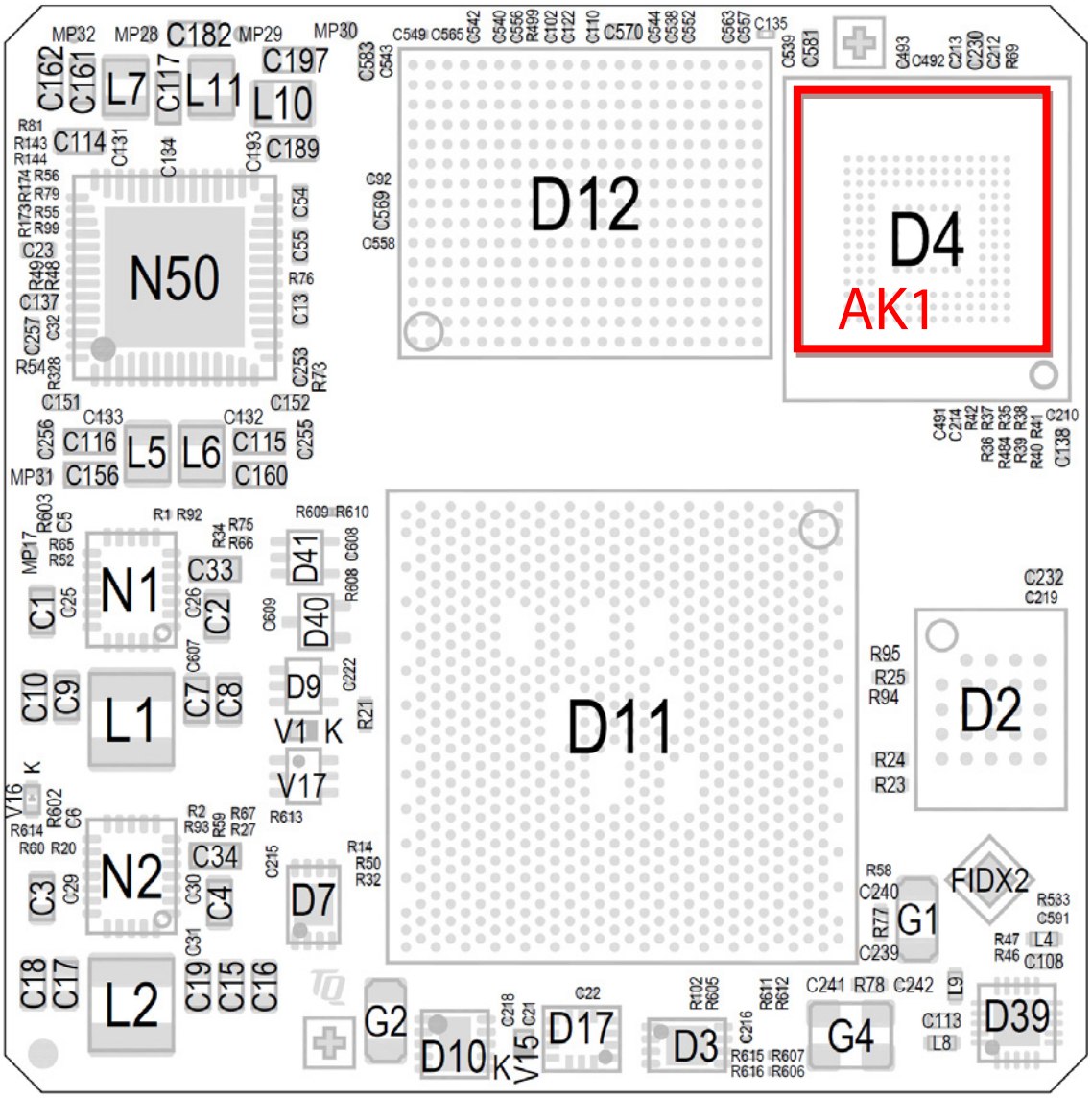

Figure 28: TQMa95xxLA, component placement top

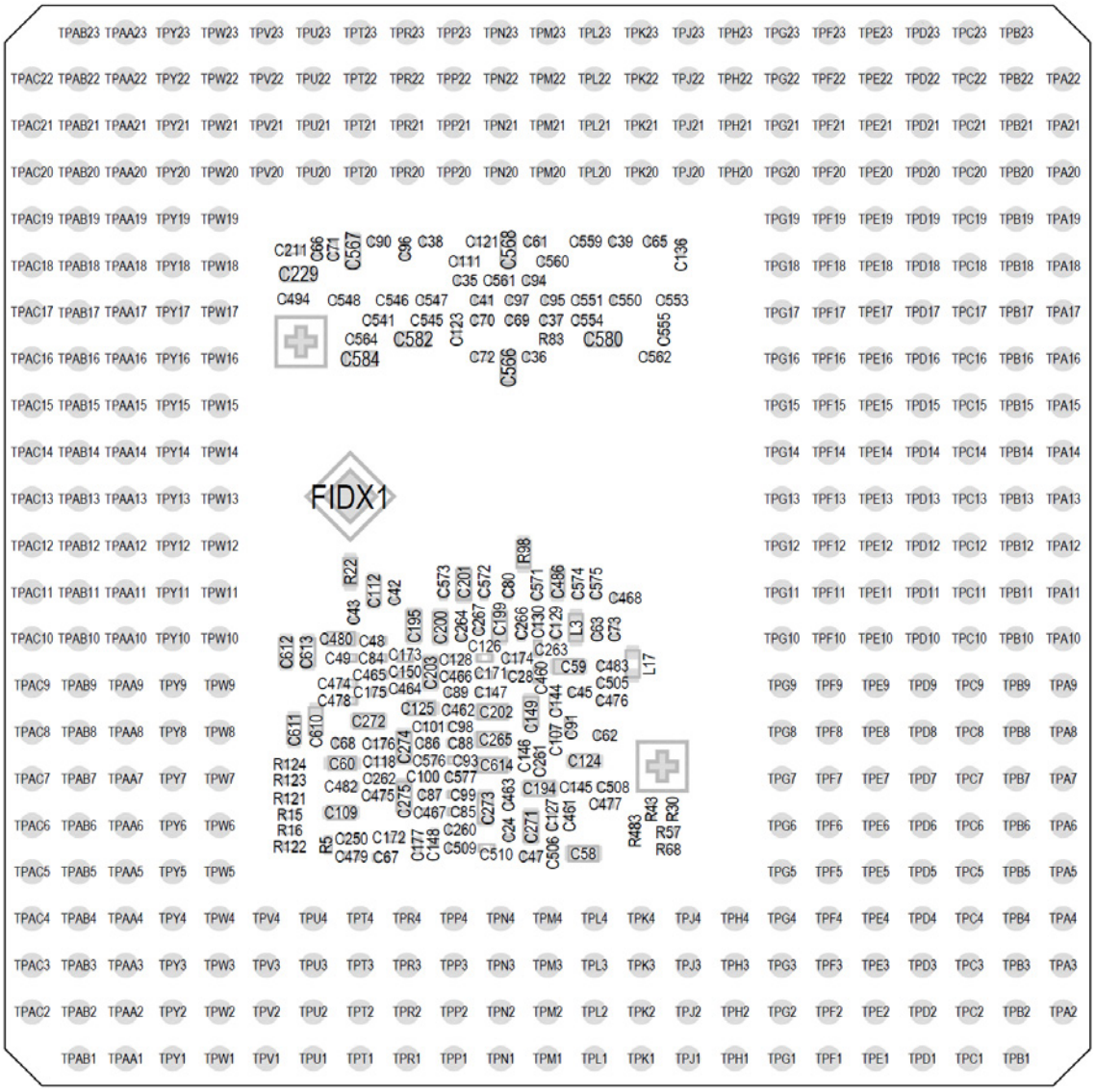

Figure 29: TQMa95xxLA, component placement bottom

The labels on the TQMa95xxLA show the following information:

Table 32: Labels on TQMa95xxLA

Label	Content
AK1	MAC address, TQMa95xxLA version and revision, serial number

4.3 Adaptation to the environment

The TQMa95xxLA has overall dimensions (length × width) of 44 mm × 44 mm (± 0.1 mm).
The TQMa95xxLA (bare die version) has a minimum height above the carrier board of 3.21 mm (±0.24 mm).
The TQMa95xxLA weighs approximately TBD.

4.4 Protection against external effects

As an embedded module, the TQMa95xxLA is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.5 Thermal management

To cool the TQMa95xxLA, a maximum of approximately TBD watts must be dissipateds.
The cooling solution must be able to dissipate this power peak; it will never occur permanently in normal operation.
The power dissipation originates primarily in the i.MX 95, the SDRAM and the PMICs.
The power dissipation also depends on the software used and can vary according to the application.
See i.MX 95 Data Sheet (1) for further information.

Attention: Destruction or malfunction, TQMa95xxLA heat dissipation	
	The TQMa95xxLA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 95 must be taken into consideration when connecting the heat sink. The i.MX 95 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa95xxLA and thus malfunction, deterioration or destruction.

4.6 Structural requirements

The TQMa95xxLA has a low retention force and has to be mounted / secured according to customer requirements.
The superior system is defined by the customer depending on the usage of the TQMa95xxLA.

5. SOFTWARE

The TQMa95xxLA is delivered with a preinstalled boot loader U-Boot and the BSP provided by TQ-Systems GmbH, which is tailored for the MBa95xxCA.

The boot loader U-Boot provides TQMa95xxLA-specific as well as board-specific settings, e.g.:

- i.MX 95 configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader is used.

More information can be found in the TQ-Support Wiki for the TQMa95xxLA.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa95xxLA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs for multi-pole interfaces (e.g. LC display).

As part of the development, an EMC test was performed with the starter kit MBa95xxCA in accordance with EN55022:2010 Class A limits.

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures are provided on the TQMa95xxLA.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Climate and operational conditions

The operating temperature range for the TQMa95xxLA strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa95xxLA.
The TQMa95xxLA is available in three different variants with different temperature ranges. In general, a reliable operation is given when following conditions are met:

Table 33: Climate and operational conditions industrial temperature range

Parameter	Range	Remark
Ambient temperature	–25 °C to +85 °C	–
Extended temperature	–40 °C to +85 °C	–
Storage temperature	-40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Attention: Destruction or malfunction, TQMa95xxLA heat dissipation	
	The TQMa95xxLA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 95 must be taken into consideration when connecting the heat sink. The i.MX 95 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa95xxLA and thus malfunction, deterioration or destruction.

6.5 Reliability and service life

The calculated MTBF of the TQMa95xxLA is approximately 778085 h @ +40 °C ambient temperature, Ground, Benign.
The TQMa95xxLA is designed to be insensitive to shock and vibration.

6.6 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa95xxLA is only a sub-component of an overall system.

6.7 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship, irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.8 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.
The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa95xxLA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of technical possibilities, the TQMa95xxLA was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.
The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.
Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.
TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

7.5 EuP

The Eco Design Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa95xxLA must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the TQMa95xxLA enable compliance with EuP requirements for the TQMa95xxLA.

7.6 Battery

No batteries are assembled on the TQMa95xxLA.

7.7 Packaging

The TQMa95xxLA is delivered in reusable packaging.

7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa95xxLA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa95xxLA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))

- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 34: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
ASIL	Automotive Safety Integrity Level
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR	Double Data Rate
DNC	Do Not Connect
DP	DisplayPort
DSI	Display Serial Interface
ECC	Error-Correcting Code
eDP	embedded DisplayPort
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card
ESD	Electrostatic Discharge
eSPI	enhanced Serial Peripheral Interface
EU	European Union
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General-Purpose Input/Output
GPMC	General-Purpose Memory Controller
GPO	General-Purpose Output
GPU	Graphics Processing Unit
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IC	Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LVDS	Low-Voltage Differential Signalling
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MIPI	Mobile Industry Processor Interface
MMC	Multimedia Card
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTBF	Mean (operating) Time Between Failures

8.1 Acronyms and definitions (continued)

Table 34: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NOR	Not-Or
OD	Open-drain
OTG	On-The-Go
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
R/W	Read/Write
RAM	Random Access Memory
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protected
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDIO	Secure Digital Input/Output
SDRAM	Synchronous Dynamic Random Access Memory
SMBus	System Management Bus
SPI	Serial Peripheral Interface
TBD	To Be Determined
TSE	Trust Secure Element
UART	Universal Asynchronous Receiver / Transmitter
UM	User's Manual
USB	Universal Serial Bus
VPU	Video Processing Unit
WDT	Watchdog Timer
WEEE®	Waste Electrical and Electronic Equipment
WP	Write Protect

8.2 References

Table 35: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 95 Industrial Application Processors Data Sheet	Rev. 1, 02/2024	NXP
(2)	i.MX 95 Applications Processor Reference Manual	Rev. 1, 02/2024	NXP
(3)	i.MX 95 Mask Set Errata	Rev. A, 01/2024	NXP
(4)	PF09 - 9-channel Power Management IC	Rev. 0.4, 08.2023	NXP
(5)	i.MX 95 Hardware Developer's Guide	Rev. A, 11/2023	NXP
(6)	MBa95xxCA User's Manual	– current –	TQ-Systems
(7)	TQMa95xxLA Support-Wiki	– current –	TQ-Systems

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