TQMa8MPxL
User's Manual

TQMa8MPxL UM 0106
11.07.2024

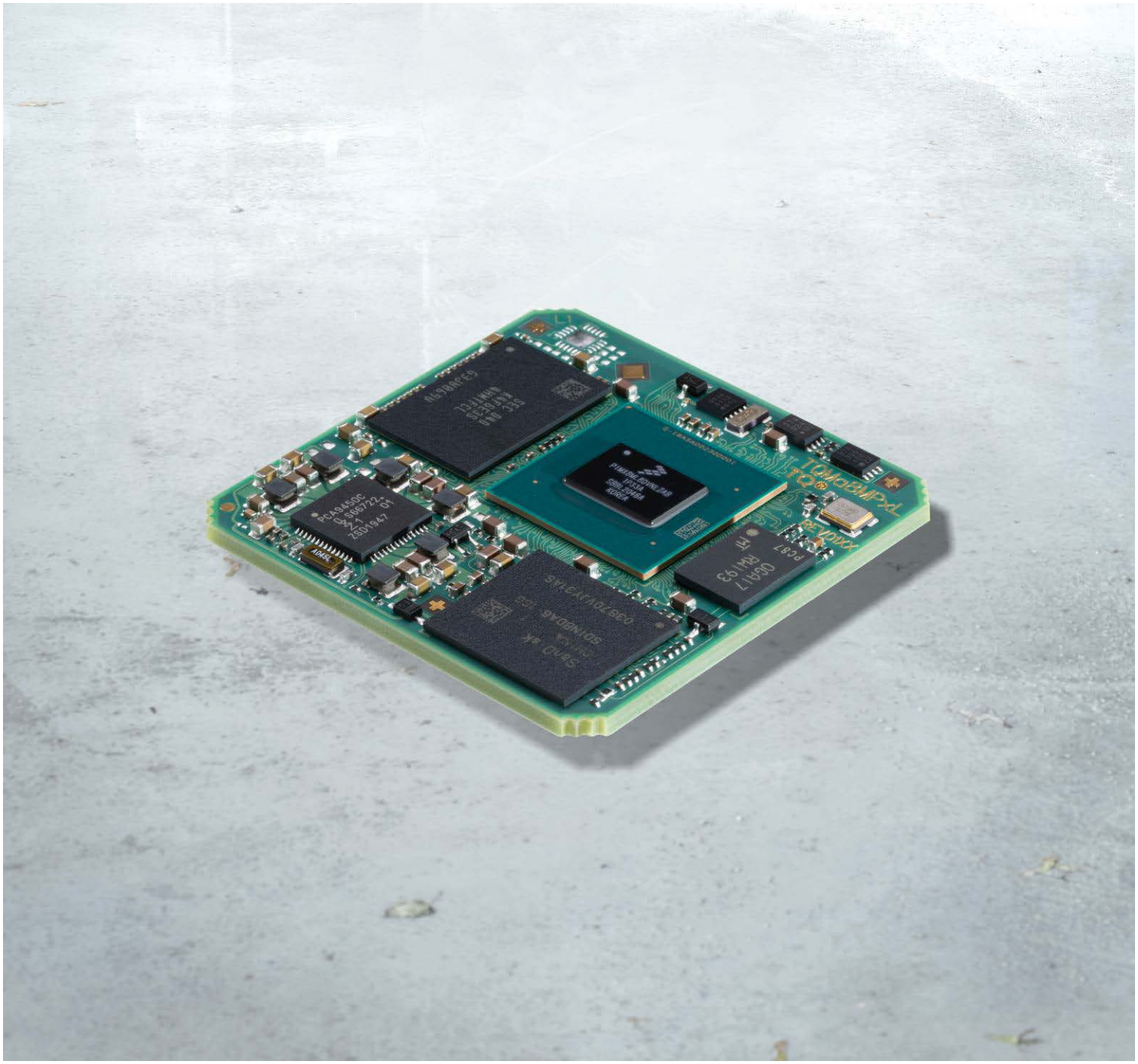

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	23.03.2022	Kreuzer		First issue
0101	22.11.2022	Kreuzer	Table 3	V_SD2 corrected to P_{out}
0102	30.05.2023	Kreuzer	Chapter 3.1.1.1	Number of pads corrected to 366
0103	20.03.2024	Kreuzer	Chapter 3.2.5.20	Chapter references corrected
0104	11.04.2024	Kreuzer	Table 3	CPU ball assignments corrected
0105	06.05.2024	Kreuzer	Table 27	Table expanded
0106	11.07.2024	Kreuzer	Figure 22, Figure 23, Figure 24 6.5	Updated to module revision 0200 Chapter added

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa8MPxL and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa8MPxL circuit diagram
- MBa8MPxL User's Manual
- i.MX 8M Plus Data Sheet
- i.MX 8M Plus Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8MPxL

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa8MPxL as of revision 0100, in combination with the MBa8MPxL as of revision 0100 and refers to some software settings. A certain TQMa8MPxL derivative does not necessarily provide all features described in this User's Manual.

This User's Manual does neither replace the i.MX 8M Plus Reference Manual (1), nor the i.MX 8M Plus Data Sheet (2), nor any other documents from NXP.

The TQMa8MPxL is a universal Minimodule based on the NXP ARM® Cortex®-A53 based i.MX 8M CPU family, see also Table 4.

2.1 Key functions and characteristics

The TQMa8MPxL extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

All essential i.MX 8M Plus signals are routed to the TQMa8MPxL LGA pads. There are therefore no restrictions for customers using the TQMa8MPxL with respect to an integrated customised design. All essential components like CPU, LPDDR4, eMMC, and PMIC are already integrated on the TQMa8MPxL.

The main features of the TQMa8MPxL are:

- 64 bit NXP i.MX 8M Plus CPU, up to 4 × ARM Cortex®-A53 and 1 × Cortex®-M7
  - Plus Dual, Plus Quad 4 Lite, Plus Quad 6 Video, Plus Quad 8 ML/AI
- Up to 4 Gbyte 32-bit LPDDR4-4000
- Up to 256 Gbyte eMMC NAND Flash, eMMC standard 5.1
- Up to 256 Mbyte QSPI NOR Flash
- 64 Kbit EEPROM (optional)
- Temperature sensor + EEPROM
- RTC (optinal)
- Trust Secure Element (optional)
- NXP Power Management Integrated Circuit PCA9450
- All essential i.MX 8M Plus signals are routed to the TQMa8MPxL LGA pads
- Single supply voltage 5 V

2.2 CPU block diagram

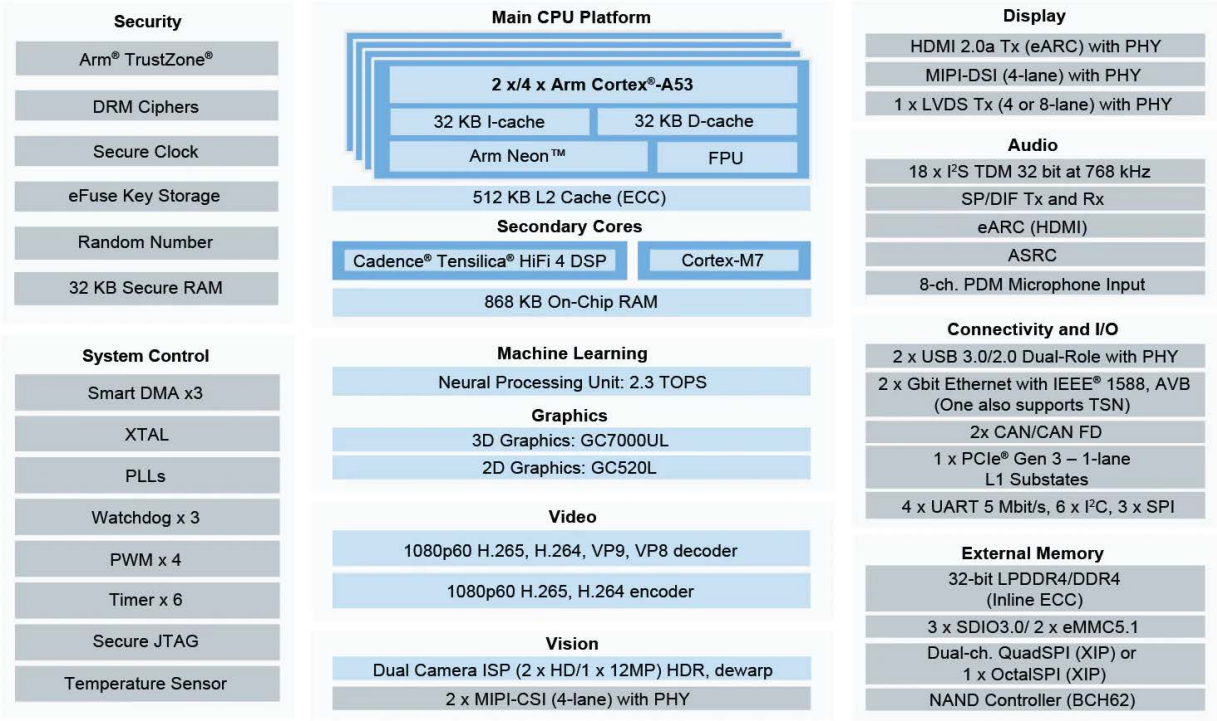


Figure 1: Block diagram i.MX 8M Plus
(Source: NXP)

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa8MPxL, and the BSP provided by TQ-Systems GmbH, see also chapter 4.

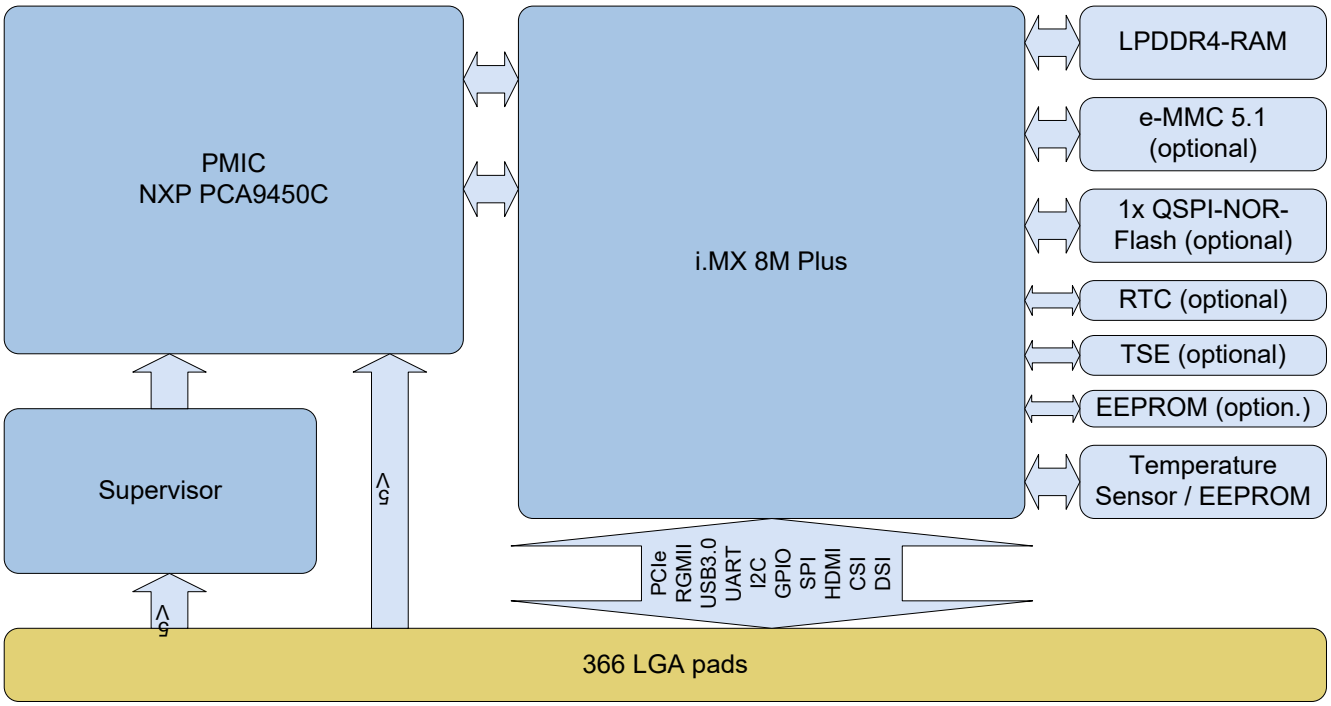


Figure 2: Block diagram TQMa8MPxL (simplified)

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

The multiple pin configurations by different i.MX 8M Plus-internal function units must be taken note of.

The pin assignment in Table 3 refers to a TQMa8MPxL with i.MX 8M Plus Quad 8 ML/AI CPU in combination with the carrier board MBa8MPxL.

NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool – NXP Tool).

The electrical and pin characteristics are to be taken from the i.MX 8M Plus and PMIC documentation, see Table 40.

Attention: Destruction or malfunction, pin multiplexing	
	Depending on the configuration, many i.MX 8M Plus pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the i.MX 8M Plus Reference Manual (1), before integration or start-up of your carrier board / Starterkit. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa8MPxL. The descriptions given in the following tables should be taken note of: – DNC: These pins must never be connected and have to be left open. Please contact TQ-Support for details.

3.1.1.1 Pinout TQMa8MPxL

The TQMa8MPxL has a total of 366 LGA pads. The TQMa8MPxL is soldered and thus permanently connected to the carrier board. It is not trivial and it is not recommended to remove the TQMa8MPxL.
The following table shows the TQMa8MPxL pad-out, top view through the TQMa8MPxL.

Table 2: Pinout TQMa8MPxL, top view through TQMa8MPxL

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	
22		USB1_D_P	USB1_D_N	GND	DSI_D1_N	DSI_D1_P	GND	DSI_D3_N	DSI_D3_P	GND	CSI1_CLK_N	CSI1_CLK_P	GND	CSI2_D0_N	CSI2_D0_P	GND	CSI2_D2_N	CSI2_D2_P	GND	PCIE_REF_CLKN	PCIE_REF_CLKP		22
21	USB1_TX_N	GND	ISO_14443_LB	ISO_14443_LA	GND	DSI_CLK_N	DSI_CLK_P	GND	CSI1_D0_N	CSI1_D0_P	GND	CSI1_D2_N	CSI1_D2_P	GND	CSI2_D1_N	CSI2_D1_P	GND	CSI2_D3_N	CSI2_D3_P	GND	PCIE_TXN	PCIE_TXP	21
20	USB1_TX_P	USB1_RX_N	GND	DSI_D0_N	DSI_D0_P	GND	DSI_D2_N	DSI_D2_P	GND	CSI1_D1_N	CSI1_D1_P	GND	CSI1_D3_N	CSI1_D3_P	GND	CSI2_CLK_N	CSI2_CLK_P	GND	PCIE_RXN	PCIE_RXP	LVDS1_D3_P	GND	20
19	GND	USB1_RX_P	USB2_D_N	USB2_DNU	GPIO1_IO11	USB1_DNU	GND	USB1_OTG_OC	ISO_7816_CLK	GND	JTAG_TDO	JTAG_TCK	GND	BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	TEMP_EVENT#	M7_NMI	GND	V_SD1	LVDS1_D3_N	LVDS1_CLK_P	19
18	USB2_TX_N	GND	USB2_D_P	GPIO1_IO15	GND	USB1_VBUS	USB1_OTG_ID	USB1_OTG_PWR	ISO_7816_IO2	ISO_7816_IO1	ISO_7816_RST	GND	JTAG_TMS	JTAG_TDI	GND	BOOT_MODE0	RTC_EVENT#	GND	CLK1_IN	GND	LVDS1_D2_P	LVDS1_CLK_N	18
17	USB2_TX_P	USB2_RX_N	GND	GPIO1_IO14	USB2_VBUS													CLK2_OUT	CLK1_OUT	LVDS1_D1_P	LVDS1_D2_N	GND	17
16	GND	USB2_RX_P	GPIO3_IO14	GND	GPIO1_IO00													GND	CLK2_IN	LVDS1_D1_N	GND	LVDS1_D0_P	16
15	V_SAI2_SAI3_SPDIF	V_SAI1_SAI5	GND	V_LICELL	GPIO1_IO01													QSPI_A_SS0#	QSPI_A_SCLK	GND	LVDS0_D3_P	LVDS1_D0_N	15
14	GND	I2C4_SCL	I2C1_SCL	GND	GPIO1_IO03													QSPI_A_DATA0	GND	LVDS0_CLK_P	LVDS0_D3_N	GND	14
13	SAI3_TXD0	I2C4_SDA	I2C2_SCL	I2C1_SDA	GND													QSPI_A_DATA1	QSPI_A_DATA2	LVDS0_CLK_N	GND	LVDS0_D2_P	13
12	SAI3_RXD0	SAI3_TXC	I2C2_SDA	GND	GPIO1_IO06													UART1_RXD	QSPI_A_DATA3	GND	LVDS0_D1_P	LVDS0_D2_N	12
11	GND	SAI3_TXFS	GND	GPIO1_IO09	GPIO1_IO07													UART1_TXD	GND	LVDS0_D0_P	LVDS0_D1_N	GND	11
10	GPIO4_IO29	GND	SAI3_MCLK	PWM3	GND													I2C6_SCL	I2C6_SDA	LVDS0_D0_N	ENET_QOS_TD3	V_ENET	10
9	GPIO4_IO28	ENET_QOS_EVENT2_IN	GPIO4_IO25	GND	GPIO5_IO27	GPIO5_IO26	RFU	GND							GND	V_SD2	GPIO2_IO07	UART2_TXD	UART2_RXD	ENET_QOS_TD2	GND	ENET_QOS_TXC	9
8	GND	ENET_QOS_EVENT2_OUT	GND	GPT2_CLK	GND	PMIC_WDOG_OUT#	GND	RFU							RFU	GND	GPIO2_IO06	UART3_RXD	GND	ENET_QOS_TX_CTL	ENET_QOS_TD0	ENET_QOS_TD1	8
7	GPIO4_IO22	GND	GPIO4_IO24	GND	RESET_IN#	RESET_OUT#	ONOFF	GND							GND	SD2_WP	SD2_RST#	UART3_TXD	GPIO2_IO11	ENET_QOS_RD3	GND	ENET_QOS_RXC	7
6	GPIO4_IO27	GPIO4_IO21	GND	GND	PMIC_RST#	PMIC_WDOG_IN#	UART4_TXD	UART4_RXD	ECSPI3_MOSI	GND	GPIO5_IO05	GPIO5_IO03	GND	ECSPI2_SS0	SD2_CD#	GND	SD2_CMD	GPIO2_IO10	GND	ENET_QOS_MDIO	ENET_QOS_RD2	GND	6
5	GND	GND	GND	GND	GND	GND	V_3V3_SD	ECSPI3_SS0	ECSPI3_MISO	ECSPI3_SCLK	GPIO5_IO04	ECSPI2_SCLK	ECSPI2_MISO	ECSPI2_MOSI	GND	SD2_DATA3	SD2_DATA2	SD2_DATA1	SD2_DATA0	ENET_QOS_MDC	GND	ENET_QOS_RD1	5
4	V_5V_IN	V_5V_IN	V_5V_IN	GND	GND	GND	ENET0_INT#	ENET1_INT#	GND	ENET0_RST#	ENET1_RST#	GND	GPIO4_IO18	ENET_RX_CTL	ENET_TX_CTL	SD2_CLK	GND	EARC_AUX	HDMI_CEC	GND	ENET_QOS_RX_CTL	ENET_QOS_RD0	4
3	V_5V_IN	V_5V_IN	V_5V_IN	GND	GND	GND	GND	ENET_MDC	ENET_MDIO	GND	ENET_RD2	ENET_RD3	GND	ENET_TD2	ENET_TD3	GND	HDMI_TXC_N	HDMI_TXC_P	GND	HDMI_HPD	GND	HDMI_DDC_SCL	3
2	GPIO3_IO20	GND	GPIO3_IO21	GPIO3_IO19	GND	GPIO5_IO09	GPIO5_IO08	GND	ENET_RD0	ENET_RD1	GND	ENET_TD0	ENET_TD1	GND	ENET_TXC	GPIO4_IO19	GND	HDMI_TX0_N	HDMI_TX0_P	HDMI_TX2_N	HDMI_TX2_P	HDMI_DDC_SDA	2
1		CAN_FD1_TX	CAN_FD1_RX	CAN_FD2_TX	CAN_FD2_RX	GND	GPIO5_IO07	GPIO5_IO06	GND	ENET_RXC	GPIO4_IO20	GND	V_1V8	V_3V3	GND	EARC_N_HPD	EARC_P_UTIL	GND	HDMI_TX1_N	HDMI_TX1_P	GND		1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	

3.1.1.2 TQMa8MPxL signals

Details about the electrical characteristics of single pins and interfaces are to be taken from the i.MX 8M Plus documentation (1), (2), (3), as well as the PMIC Data Sheet (4).

Table 3: TQMa8MPxL, signals

CPU-Ball	Signal	Group	Dir.	Level	TQMa8MPxL-Pad
G10	BOOT_MODE0	BOOT	I	3.3 V	T18
F8	BOOT_MODE1	BOOT	I	3.3 V	T19
G8	BOOT_MODE2	BOOT	I	3.3 V	R19
G12	BOOT_MODE3	BOOT	I	3.3 V	P19
AF16	CAN_FD1_RX	CAN	I	V_SAI1_SAI5	C1
AD16	CAN_FD1_TX	CAN	O	V_SAI1_SAI5	B1
AF14	CAN_FD2_RX	CAN	I	V_SAI1_SAI5	E1
AE14	CAN_FD2_TX	CAN	O	V_SAI1_SAI5	D1
K28	CLK1_IN	CLK	I	1.8 V	W18
K29	CLK1_OUT	CLK	O	1.8 V	W17
L28	CLK2_IN	CLK	I	1.8 V	W16
L29	CLK2_OUT	CLK	O	1.8 V	V17
E22	CSI1_CLK_N	CSI	I	1.8 V	L22
D22	CSI1_CLK_P	CSI	I	1.8 V	M22
E18	CSI1_D0_N	CSI	I	1.8 V	J21
D18	CSI1_D0_P	CSI	I	1.8 V	K21
E20	CSI1_D1_N	CSI	I	1.8 V	K20
D20	CSI1_D1_P	CSI	I	1.8 V	L20
E24	CSI1_D2_N	CSI	I	1.8 V	M21
D24	CSI1_D2_P	CSI	I	1.8 V	N21
E26	CSI1_D3_N	CSI	I	1.8 V	N20
D26	CSI1_D3_P	CSI	I	1.8 V	P20
B23	CSI2_CLK_N	CSI	I	1.8 V	T20
A23	CSI2_CLK_P	CSI	I	1.8 V	U20
B25	CSI2_D0_N	CSI	I	1.8 V	P22
A25	CSI2_D0_P	CSI	I	1.8 V	R22
B24	CSI2_D1_N	CSI	I	1.8 V	R21
A24	CSI2_D1_P	CSI	I	1.8 V	T21
B22	CSI2_D2_N	CSI	I	1.8 V	U22
A22	CSI2_D2_P	CSI	I	1.8 V	V22
B21	CSI2_D3_N	CSI	I	1.8 V	V21
A21	CSI2_D3_P	CSI	I	1.8 V	W21
B18	DSI_CLK_N	DSI	O	1.8 V	F21
A18	DSI_CLK_P	DSI	O	1.8 V	G21
B16	DSI_D0_N	DSI	O	1.8 V	D20
A16	DSI_D0_P	DSI	O	1.8 V	E20
B17	DSI_D1_N	DSI	O	1.8 V	E22
A17	DSI_D1_P	DSI	O	1.8 V	F22
B19	DSI_D2_N	DSI	O	1.8 V	G20
A19	DSI_D2_P	DSI	O	1.8 V	H20
B20	DSI_D3_N	DSI	O	1.8 V	H22
A20	DSI_D3_P	DSI	O	1.8 V	J22

3.1.1.2 TQMa8MPxL signals (continued)

Table 3: TQMa8MPxL, signals (continued)

CPU	Signal	Group	Dir.	Level	TQMa8MPxL
AH20	ECSPI2_MISO	ECSPI	I	1.8 V	N5
AJ21	ECSPI2_MOSI	ECSPI	O	1.8 V	P5
AH21	ECSPI2_SCLK	ECSPI	O	1.8 V	M5
AJ22	ECSPI2_SS0	ECSPI	O	1.8 V	P6
AF6	ECSPI3_MISO	ECSPI	I	3.3 V	J5
AJ3	ECSPI3_MOSI	ECSPI	O	3.3 V	J6
AD6	ECSPI3_SCLK	ECSPI	O	3.3 V	K5
AH4	ECSPI3_SS0	ECSPI	O	3.3 V	H5
AJ9	ENET0_RST#	ENET	O	V_SAI1_SAI5	K4
AH8	ENET0_INT#	ENET	I	V_SAI1_SAI5	G4
AC10	ENET1_RST#	ENET	O	V_SAI1_SAI5	L4
AF10	ENET1_INT#	ENET	I	V_SAI1_SAI5	H4
AH9	ENET_MDC	ENET	O	V_SAI1_SAI5	H3
AJ8	ENET_MDIO	ENET	I/O	V_SAI1_SAI5	J3
AH28	ENET_QOS_MDC	ENET	O	V_ENET	Y5
AH29	ENET_QOS_MDIO	ENET	I/O	V_ENET	Y6
AG29	ENET_QOS_RD0	ENET	I	V_ENET	AB4
AG28	ENET_QOS_RD1	ENET	I	V_ENET	AB5
AF29	ENET_QOS_RD2	ENET	I	V_ENET	AA6
AF28	ENET_QOS_RD3	ENET	I	V_ENET	Y7
AE28	ENET_QOS_RX_CTL	ENET	I	V_ENET	AA4
AE29	ENET_QOS_RXC	ENET	I	V_ENET	AB7
AC25	ENET_QOS_TD0	ENET	O	V_ENET	AA8
AE26	ENET_QOS_TD1	ENET	O	V_ENET	AB8
AF26	ENET_QOS_TD2	ENET	O	V_ENET	Y9
AD24	ENET_QOS_TD3	ENET	O	V_ENET	AA10
AF24	ENET_QOS_TX_CTL	ENET	O	V_ENET	Y8
AE24	ENET_QOS_TXC	ENET	O	V_ENET	AB9
AJ14	ENET_QOS_EVENT2_OUT	ENET	O	V_SAI2_SAI3_SPDIF	B8
AH16	ENET_QOS_EVENT2_IN	ENET	I	V_SAI2_SAI3_SPDIF	B9
AD10	ENET_RD0	ENET	I	V_SAI1_SAI5	J2
AE10	ENET_RD1	ENET	I	V_SAI1_SAI5	K2
AH10	ENET_RD2	ENET	I	V_SAI1_SAI5	L3
AH12	ENET_RD3	ENET	I	V_SAI1_SAI5	M3
AF12	ENET_RX_CTL	ENET	I	V_SAI1_SAI5	P4
AJ12	ENET_RXC	ENET	I	V_SAI1_SAI5	K1
AJ11	ENET_TD0	ENET	O	V_SAI1_SAI5	M2
AJ10	ENET_TD1	ENET	O	V_SAI1_SAI5	N2
AH11	ENET_TD2	ENET	O	V_SAI1_SAI5	P3
AD12	ENET_TD3	ENET	O	V_SAI1_SAI5	R3
AE12	ENET_TX_CLK	ENET	O	V_SAI1_SAI5	L1
AH13	ENET_TX_CTL	ENET	O	V_SAI1_SAI5	R4
AH14	ENET_TXC	ENET	O	V_SAI1_SAI5	R2
B4	M7_NMI	Event	I	3.3 V	V19
-	RTC_EVENT#	Event	O	OD	U18
-	TEMP_EVENT#	Event	O	OD	U19

3.1.1.2 TQMa8MPxL signals (continued)

Table 3: TQMa8MPxL, signals (continued)

CPU	Signal	Group	Dir.	Level	TQMa8MPxL
A7	GPIO1_IO00	GPIO	I/O	3.3 V	E16
E8	GPIO1_IO01	GPIO	I/O	3.3 V	E15
D6	GPIO1_IO03	GPIO	I/O	3.3 V	E14
A3	GPIO1_IO06	GPIO	I/O	3.3 V	E12
F6	GPIO1_IO07	GPIO	I/O	3.3 V	E11
B8	GPIO1_IO09	GPIO	I/O	3.3 V	D11
D8	GPIO1_IO11	GPIO	I/O	3.3 V	E19
A4	GPIO1_IO14	GPIO	I/O	3.3 V	D17
B5	GPIO1_IO15	GPIO	I/O	3.3 V	D18
U26	GPIO2_IO06	GPIO	I/O	V_SD1	U8
AA29	GPIO2_IO07	GPIO	I/O	V_SD1	U9
W25	GPIO2_IO10	GPIO	I/O	V_SD1	V6
W26	GPIO2_IO11	GPIO	I/O	V_SD1	W7
R26	GPIO3_IO14	GPIO	I/O	1.8 V	C16
AC14	GPIO3_IO19	GPIO	I/O	V_SAI1_SAI5	D2
AD14	GPIO3_IO20	GPIO	I/O	V_SAI1_SAI5	A2
AE16	GPIO3_IO21	GPIO	I/O	V_SAI1_SAI5	C2
AC12	GPIO4_IO18	GPIO	I/O	V_SAI1_SAI5	N4
AJ13	GPIO4_IO19	GPIO	I/O	V_SAI1_SAI5	T2
AH17	GPIO4_IO21	GPIO	I/O	V_SAI2_SAI3_SPDIF	B6
AJ16	GPIO4_IO22	GPIO	I/O	V_SAI2_SAI3_SPDIF	A7
AJ17	GPIO4_IO24	GPIO	I/O	V_SAI2_SAI3_SPDIF	C7
AH15	GPIO4_IO25	GPIO	I/O	V_SAI2_SAI3_SPDIF	C9
AJ15	GPIO4_IO27	GPIO	I/O	V_SAI2_SAI3_SPDIF	A6
AJ19	GPIO4_IO28	GPIO	I/O	V_SAI2_SAI3_SPDIF	A9
AJ18	GPIO4_IO29	GPIO	I/O	V_SAI2_SAI3_SPDIF	A10
AE18	GPIO5_IO03	GPIO	I/O	V_SAI2_SAI3_SPDIF	M6
AD18	GPIO5_IO04	GPIO	I/O	V_SAI2_SAI3_SPDIF	L5
AC18	GPIO5_IO05	GPIO	I/O	V_SAI2_SAI3_SPDIF	L6
AF20	GPIO5_IO06	GPIO	I/O	1.8 V	H1
AC20	GPIO5_IO07	GPIO	I/O	1.8 V	G1
AD20	GPIO5_IO08	GPIO	I	1.8 V	G2
AE20	GPIO5_IO09	GPIO	O	1.8 V	F2
AJ4	GPIO5_IO27	GPIO	I/O	3.3 V	E9
AE6	GPIO5_IO26	GPIO	I/O	3.3 V	F9
AJ7	GPT2_CLK	GPT	I/O	3.3 V	D8
AH23	EARC_AUX	HDMI	O	1.8 V	V4
AH22	EARC_N_HPD	HDMI	I	1.8 V	T1
AJ23	EARC_P_UTIL	HDMI	O	1.8 V	U1
AD22	HDMI_CEC	HDMI	O	1.8 V	W4
AC22	HDMI_DDC_SCL	HDMI	O	1.8 V	AB3
AF22	HDMI_DDC_SDA	HDMI	I/O	1.8 V	AB2
AE22	HDMI_HPD	HDMI	I	1.8 V	Y3
AJ25	HDMI_TX0_N	HDMI	O	1.8 V	V2
AH25	HDMI_TX0_P	HDMI	O	1.8 V	W2
AJ26	HDMI_TX1_N	HDMI	O	1.8 V	W1

3.1.1.2 TQMa8MPxL signals (continued)

Table 3: TQMa8MPxL, signals (continued)

CPU	Signal	Group	Dir.	Level	TQMa8MPxL
AH26	HDMI_TX1_P	HDMI	O	1.8 V	Y1
AJ27	HDMI_TX2_N	HDMI	O	1.8 V	Y2
AH27	HDMI_TX2_P	HDMI	O	1.8 V	AA2
AJ24	HDMI_TXC_N	HDMI	O	1.8 V	U3
AH24	HDMI_TXC_P	HDMI	O	1.8 V	V3
AC8	I2C1_SCL	I2C	O	3.3 V	C14
AH7	I2C1_SDA	I2C	I/O	3.3 V	D13
AH6	I2C2_SCL	I2C	O	3.3 V	C13
AE8	I2C2_SDA	I2C	I/O	3.3 V	C12
AF8	I2C4_SCL	I2C	O	3.3 V	B14
AD8	I2C4_SDA	I2C	I/O	3.3 V	B13
Y29	I2C6_SCL	I2C	O	V_SD1	V10
Y28	I2C6_SDA	I2C	I/O	V_SD1	W10
-	ISO_7816_CLK	ISO_7816	I	3.3 V	J19
-	ISO_7816_IO1	ISO_7816	I/O	3.3 V	K18
-	ISO_7816_IO2	ISO_7816	I/O	3.3 V	J18
-	ISO_7816_RST	ISO_7816	I	3.3 V	L18
-	ISO_14443_LA	ISO_14443	I/O	3.3 V	D21
-	ISO_14443_LB	ISO_14443	I/O	3.3 V	C21
G18	JTAG_TCK	JTAG	I	3.3 V	M19
G16	JTAG_TDI	JTAG	I	3.3 V	P18
F14	JTAG_TDO	JTAG	O	3.3 V	L19
G14	JTAG_TMS	JTAG	I	3.3 V	N18
G28	LVDS0_CLK_N	LVDS	O	1.8 V	Y13
F29	LVDS0_CLK_P	LVDS	O	1.8 V	Y14
E28	LVDS0_D0_N	LVDS	O	1.8 V	Y10
D29	LVDS0_D0_P	LVDS	O	1.8 V	Y11
F28	LVDS0_D1_N	LVDS	O	1.8 V	AA11
E29	LVDS0_D1_P	LVDS	O	1.8 V	AA12
H28	LVDS0_D2_N	LVDS	O	1.8 V	AB12
G29	LVDS0_D2_P	LVDS	O	1.8 V	AB13
J28	LVDS0_D3_N	LVDS	O	1.8 V	AA14
H29	LVDS0_D3_P	LVDS	O	1.8 V	AA15
B28	LVDS1_CLK_N	LVDS	O	1.8 V	AB18
A28	LVDS1_CLK_P	LVDS	O	1.8 V	AB19
B26	LVDS1_D0_N	LVDS	O	1.8 V	AB15
A26	LVDS1_D0_P	LVDS	O	1.8 V	AB16
B27	LVDS1_D1_N	LVDS	O	1.8 V	Y16
A27	LVDS1_D1_P	LVDS	O	1.8 V	Y17
C28	LVDS1_D2_N	LVDS	O	1.8 V	AA17
B29	LVDS1_D2_P	LVDS	O	1.8 V	AA18
D28	LVDS1_D3_N	LVDS	O	1.8 V	AA19
C29	LVDS1_D3_P	LVDS	O	1.8 V	AA20

3.1.1.2 TQMa8MPxL signals (continued)

Table 3: TQMa8MPxL, signals (continued)

CPU	Signal	Group	Dir.	Level	TQMa8MPxL
E16	PCIE_REF_CLKN	PCIe	I/O	1.8 V	Y22
D16	PCIE_REF_CLKP	PCIe	I/O	1.8 V	AA22
B14	PCIE_RXN	PCIe	I	1.8 V	W20
A14	PCIE_RXP	PCIe	I	1.8 V	Y20
B15	PCIE_TXN	PCIe	O	1.8 V	AA21
A15	PCIE_TXP	PCIe	O	1.8 V	AB21
AJ6	PWM3	PWM	O	3.3 V	D10
R25	QSPI_A_DATA0	QSPI	I/O	1.8 V	V14
L25	QSPI_A_DATA1	QSPI	I/O	1.8 V	V13
L24	QSPI_A_DATA2	QSPI	I/O	1.8 V	W13
N24	QSPI_A_DATA3	QSPI	I/O	1.8 V	W12
N25	QSPI_A_SCLK	QSPI	O	1.8 V	W15
L26	QSPI_A_SS0#	QSPI	O	1.8 V	V15
-	PMIC_RST#	Reset	I	1.8 V	E6
-	PMIC_WDOG_IN#	Reset	I	3.3 V	F6
B6	PMIC_WDOG_OUT#	Reset	O	3.3 V	F8
-	RESET_IN#	Reset	I	OD	E7
-	RESET_OUT#	Reset	O	OD	F7
AJ20	SAI3_MCLK	SAI	O	V_SAI2_SAI3_SPDIF	C10
AF18	SAI3_RXD0	SAI	I	V_SAI2_SAI3_SPDIF	A12
AC16	SAI3_TXFS	SAI	O	V_SAI2_SAI3_SPDIF	B11
AH19	SAI3_TXC	SAI	O	V_SAI2_SAI3_SPDIF	B12
AH18	SAI3_TXD0	SAI	O	V_SAI2_SAI3_SPDIF	A13
AD29	SD2_CD#	SD	I	1.8/ 3.3 V	R6
AB29	SD2_CLK	SD	O	1.8/ 3.3 V	T4
AB28	SD2_CMD	SD	I/O	1.8/ 3.3 V	U6
AC28	SD2_DATA0	SD	I/O	1.8/ 3.3 V	W5
AC29	SD2_DATA1	SD	I/O	1.8/ 3.3 V	V5
AA26	SD2_DATA2	SD	I/O	1.8/ 3.3 V	U5
AA25	SD2_DATA3	SD	I/O	1.8/ 3.3 V	T5
AD28	SD2_RST#	SD	O	1.8/ 3.3 V	U7
AC26	SD2_WP	SD	I	1.8/ 3.3 V	T7

3.1.1.2 TQMa8MPxL signals (continued)

Table 3: TQMa8MPxL, signals (continued)

CPU	Signal	Group	Dir.	Level	TQMa8MPxL
G22	ONOFF	SNVS	I	1.8 V	G7
W29	UART1_RXD	UART	I	V_SD1	V12
W28	UART1_TXD	UART	O	V_SD1	V11
V28	UART2_RXD	UART	I	V_SD1	W9
V29	UART2_TXD	UART	O	V_SD1	V9
U25	UART3_RXD	UART	I	V_SD1	V8
AA28	UART3_TXD	UART	O	V_SD1	V7
AJ5	UART4_RXD	UART	I	3.3 V	H6
AH5	UART4_TXD	UART	O	3.3 V	G6
E10	USB1_D_N	USB	I/O	3.3 V	C22
D10	USB1_D_P	USB	I/O	3.3 V	B22
B11	USB1_DNU	USB	–	3.3 V	F19
B7	USB1_OTG_ID	USB	I	3.3 V	G18
A6	USB1_OTG_OC	USB	I	3.3 V	H19
A5	USB1_OTG_PWR	USB	O	3.3 V	H18
B9	USB1_RX_N	USB	I	3.3 V	B20
A9	USB1_RX_P	USB	I	3.3 V	B19
B10	USB1_TX_N	USB	O	3.3 V	A21
A10	USB1_TX_P	USB	O	3.3 V	A20
A11	USB1_VBUS	USB	P	5 V	F18
E14	USB2_D_N	USB	I/O	3.3 V	C19
D14	USB2_D_P	USB	I/O	3.3 V	C18
E12	USB2_DNU	USB	–	3.3 V	D19
B12	USB2_RX_N	USB	I	3.3 V	B17
A12	USB2_RX_P	USB	I	3.3 V	B16
B13	USB2_TX_N	USB	O	3.3 V	A18
A13	USB2_TX_P	USB	O	3.3 V	A17
D12	USB2_VBUS	USB	P	5 V	E17
–	GND	A11, A14, A16, A19, A5, A8, AA1, AA13, AA16, AA3, AA5, AA7, AA9, AB11, AB14, AB17, AB20, AB6, B10, B18, B2, B21, B5, B7, C11, C15, C17, C20, C5, C6, C8, D12, D14, D16, D22, D3, D4, D5, D6, D7, D9, E10, E13, E18, E2, E21, E3, E4, E5, E8, F1, F20, F3, F4, F5, G19, G22, G3, G8, H2, H21, H7, H9, J1, J20, J4, K19, K22, K3, K6, L2, L21, M1, M18, M20, M4, N19, N22, N3, N6, P2, P21, R1, R18, R20, R5, R7, R9, T22, T3, T6, T8, U2, U21, U4, V1, V16, V18, V20, W11, W14, W19, W22, W3, W6, W8, Y12, Y15, Y18, Y21, Y4				
-	V_1V8	Power	P_{out}	1.8 V [1]	N1
-	V_3V3	Power	P_{out}	3.3 V [1]	P1
-	V_3V3_SD	Power	P_{out}	3.3 V [2]	G5
-	V_5V_IN	Power	P_{in}	5 V	A3, A4, B3, B4, C3, C4
AA24	V_ENET	Power	P_{in}	1.8 / 3.3 V	AB10
-	V_LICELL	Power	P_{in}	3 V	D15
Y11	V_SAI1_SAI5	Power	P_{in}	1.8 / 3.3 V	B15
AA11	V_SAI2_SAI3_SPDIF	Power	P_{in}	1.8 / 3.3 V	A15
U24	V_SD1	Power	P_{in}	1.8 / 3.3 V	Y19
-	V_SD2	Power	P_{out}	1.8 / 3.3 V	T9
-	RFU	Reserved for future use. Do not connect.			G9, H8, R8

1: Maximum load of 500 mA.
2: Maximum load of 400 mA.

3.2 System components

3.2.1 i.MX 8M Plus

3.2.1.1 i.MX 8M Plus derivatives

Depending on the TQMa8MPxL version, one of the following i.MX 8M Plus derivatives is assembled.

Table 4: i.MX 8M Plus derivatives

TQMa8MPxL version	i.MX 8M Plus derivative	i.MX 8M Plus clocks	Temperature range
TQMa8MPDL-XX	i.MX 8M Plus Dual	A53: 1.6 GHz, M7: 800 MHz	–40 °C … +105 °C
TQMa8MPQLL-AA	i.MX 8M Plus Quad 4 Lite	A53: 1.6 GHz, M7: 800 MHz	–40 °C … +105 °C
TQMa8MPQL-AA	i.MX 8M Plus Quad 6 Video	A53: 1.6 GHz, M7: 800 MHz	–40 °C … +105 °C
TQMa8MPQL-AB	i.MX 8M Plus Quad 8 ML/AI	A53: 1.6 GHz, M7: 800 MHz	–40 °C … +105 °C

3.2.1.2 i.MX 8M Plus errata

Attention: Destruction or malfunction, i.MX 8M Plus errata	
	Please take note of the current i.MX 8M Plus errata (5).

3.2.1.3 Boot modes

The i.MX 8M Plus has a ROM with integrated boot loader. After the release of PMIC_POR# the System Controller (SCU) boots from the internal ROM and then loads the program image from the selected boot device. For example, the integrated eMMC or the optional QSPI NOR Flash can be selected as the default boot device. The following boot sources are supported by TQMa8MPxL:

- eMMC
- QSPI NOR Flash
- USB OTG
- SD card

Alternatively, an image can be loaded into the internal RAM using the serial downloader.

More information about the boot flow can be found in the Reference Manual (1), and the Data Sheet (2) of i.MX 8M Plus.

3.2.1.4 Boot configuration

The i.MX 8M Plus uses four BOOT_MODE signals available on the TQMa8MPxL's LGA pads. These require pull-up/pull-down wiring to 3.3 V and Ground. The exact boot behaviour depends on the BT_FUSE_SEL register value.

Booting from USDHC1 is only possible on the i.MX 8M Plus after burning the eFuses.

The following table shows the behaviour in dependence of BT_FUSE_SEL and selected boot mode:

Table 5: Boot configuration i.MX 8M Plus

Boot source	BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0
Boot from eFuse	0	0	0	0
USB Serial Downloader	0	0	0	1
Boot from USDHC3 (eMMC)	0	0	1	0
Boot from USDHC2 (SD card)	0	0	1	1
Boot from NAND (not supported)	0	1	0	x
Boot from QSPI (3 Byte Read)	0	1	1	0
Boot from QSPI (Hyperflash) (not supported)	0	1	1	1
Boot from eCSPI (not supported)	1	0	0	0
(Reserved)	1	0	0	1

3.2.2 Memory

3.2.2.1 LPDDR4 SDRAM

The memory interface of the i.MX 8M Plus supports DDR4 and LPDDR4 memory (32 bit bus) with a maximum clock rate of 2.0 GHz, which meets JEDEC LPDDR4-4000 standard. The TQMa8MPxL exclusively uses LPDDR4. A maximum of 8 Gbyte of LPDDR4 SDRAM is supported.

3.2.2.2 eMMC

An eMMC is provided on the TQMa8MPxL for boot loader, operating system and application software. It is connected to the i.MX 8M Plus via USDHC3.

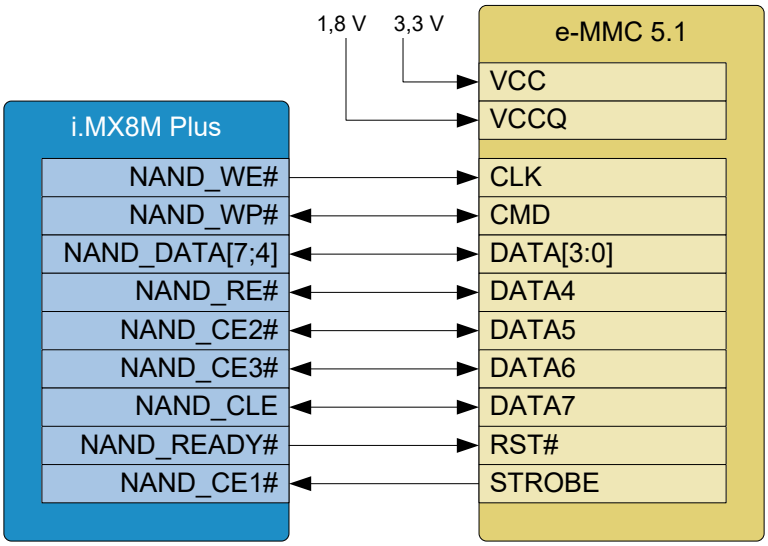


Figure 3: Block diagram eMMC

The i.MX 8M Plus supports transfer modes up to the current eMMC standard v5.1 according to JESD84-B51. In DDR mode (HS400) data rates of up to 400 Mbyte/s can be achieved.
The boot configuration is described in chapter 3.2.1.3

3.2.2.3 QSPI NOR Flash

QSPI NOR flash can optionally be assembled on the TQMa8MPxL.
If no QSPI NOR Flash is populated on the TQMa8MPxL, the LGA pads of the interface can be used. Since it is not possible to separate the signal paths, these LGA pads must not be wired when the NOR Flash is equipped.

3.2.2.4 EEPROM 24LC64T

A serial EEPROM, controlled by the I2C1 bus, is assembled. Write-Protection (WP) is not supported.
A 64 Kbit EEPROM 24LC64T is assembled by default on the TQMa8MPxL.

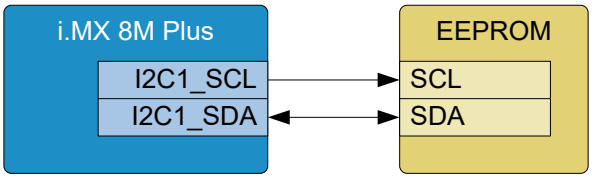


Figure 4: Block diagram EEPROM

- The EEPROM has I²C address `0x57 / 101 0111b`

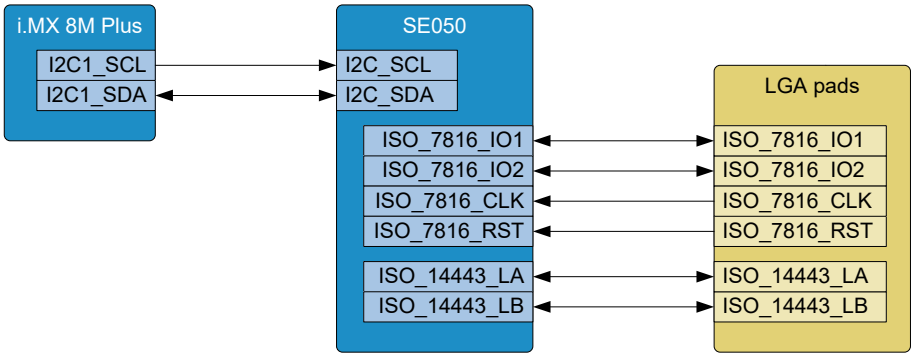
3.2.2.5 EEPROM with temperature sensor SE97BTP

A serial EEPROM including temperature sensor type SE97BTP, controlled by the I2C1 bus, is assembled on the TQMa8MPxL.
The lower 128 bytes (address 00h to 7Fh) can be set to Permanent Write-Protected mode (PWP) or to Reversible Write-Protected mode (RWP) by software. The upper 128 bytes (address 80h to FFh) cannot be write-protected and are available for general data storage.
The overtemperature output of the SE97BTP is connected as open drain to TQMa8MPxL LGA pad U19 (TEMP_EVENT#). This requires a pull-up to 3.3 V (maximum 5.5 V) on the carrier board.
The device is assembled on the top side of the TQMa8MPxL, see component D12, Figure 22.

- The device provides the following I2C addresses:
  - EEPROM (Normal Mode): `0x53 / 101 0011b`
  - EEPROM (Protection Mode): `0x33 / 011 0011b`
  - Temperature sensor: `0x1B / 001 1011b`

3.2.3 Trust Secure Element SE050

An NXP Trust Secure Element SE050 is available on the TQMa8MPxL as an assembly option. When equipped, the chip provides two interfaces according to ISO 7816 and ISO 14443. Among other things, antennas can be connected to these.



The SE050 is controlled by the I2C1 bus. More details can be found in (8).

- The Trust Secure Element has I²C address `0x48 / 100 1000b`

3.2.4 RTC

The TQMa8MPxL provides an i.MX 8M Plus-internal RTC or a discrete RTC PCF85063A.

3.2.4.1 i.MX 8M Plus internal RTC

The i.MX 8M Plus provides an RTC, which has its own power domain (V_1V8_SNVS). The RTC power domain SNVS of the i.MX 8M Plus is supplied by the PMIC. The PMIC is supplied by the TQMa8MPxL input voltage of V_5V_IN.
The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

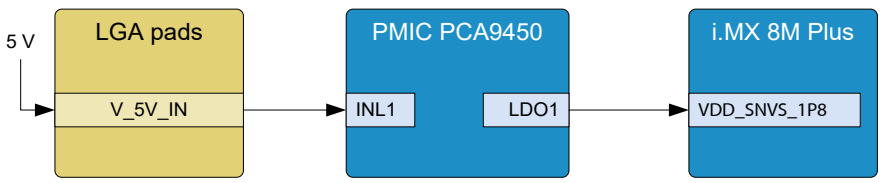


Figure 5: Block diagram RTC supply (TQMa8MPxL without discrete RTC)

Note: RTC power supply	
	The CPU internal RTC can be used in regular operation. If the TQMa8MPxL supply (5 V) fails, it is no longer available, since the i.MX 8M Plus's SNVS rail is no longer supplied.

3.2.4.2 Discrete RTC PCF85063A

In addition to the i.MX 8M Plus internal RTC the TQMa8MPxL provides a discrete RTC PCF85063A as an assembly option, which is controlled by the I2C1 bus. The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

The discrete RTC has an interrupt output which provides the open-drain signal RTC_EVENT# at LGA pad U18.

This pin requires a pull-up to 3.3 V (maximum 3.6 V) on the carrier board.

The RTC PCF85063A is only directly supplied by V_LICELL when the PMIC or the TQMa8MPxL supply is switched off.

During normal operation of the TQMa8MPxL, the PMIC supplies 3.3 V.

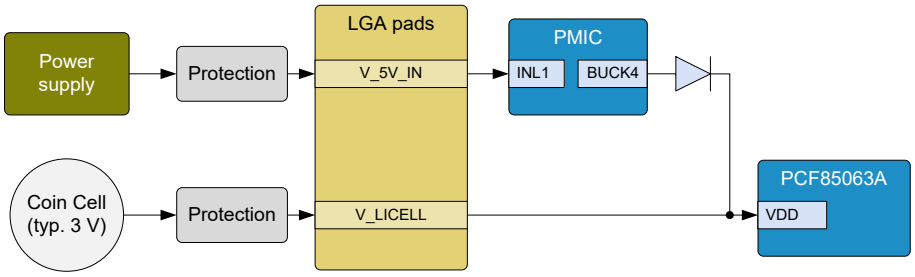


Figure 6: Block diagram RTC supply (TQMa8MPxL with discrete RTC)

➢ The discrete RTC has I2C address `0x51 / 101 0001b`

Note: RTC power supply	
	The SNVS functions of the i.MX 8M Plus can only be used if the TQMa8MPxL is supplied with 5 V. Since the SNVS rail is not supplied when the TQMa8MPxL is not powered-up, we recommend using the optional RTC PCF85063A.

3.2.5 Interfaces

3.2.5.1 Overview

The following interfaces or signals are not available on the TQMa8MPxL LGA pads and are used on the TQMa8MPxL.

Table 6: TQMa8MPxL-internal interfaces

Interface	Chapter	Remark
USDHC3	3.2.2.2	eMMC, 8 bit
SDRAM	3.2.2.1	LPDDR4, 32 bit
GPIO1_IO04 / SD2_VSELECT	3.2.5.20	–
GPIO1_IO08 / IRQ#	–	100 kΩ PU on TQMa8MPxL
POR#	–	100 kΩ PU on TQMa8MPxL, signal from CPU to PMIC
PMIC_ON_REQ	–	Signal from CPU to PMIC
PMIC_STBY_REQ	–	Signal from CPU to PMIC
RTC_XTALO	–	100 kΩ PU on TQMa8MPxL

3.2.5.2 CAN FD

The i.MX 8M Plus provides two CAN FD interfaces, CAN FD1 and CAN FD2. Both are multiplexed to SAI5 pins in the standard configuration and specified according to the CAN 2.0B protocol. The supply voltage is set via TQMa8MPxL LGA pad V_SAI1_SAI5.

Table 7: CAN FD signals

Signal	i.MX 8M Plus	TQMa8MPxL	Power group
CAN_FD1_TX	AD16	B1	V_SAI1_SAI5
CAN_FD1_RX	AF16	C1	
CAN_FD2_TX	AE14	D1	
CAN_FD2_RX	AF14	E1	

3.2.5.3 PWM

The i.MX 8M Plus provides up to four PWM signals which can be multipexed via various pins. In the default configuration one PWM signal (PWM3) is provided at the TQMa8MPxL LGA pad D10.

3.2.5.4 GPT

The i.MX 8M Plus provides up to three General Purpose Timers (GPT). These always use a part of the UART res. I2C pins of the CPU. Therefore only the GPT2 interface (GPT2_CLK) is provided by the TQMa8MPxL pad D8.

3.2.5.5 Ethernet

The i.MX 8M Plus provides two Gigabit Ethernet interfaces, which support transfer rates of 10/100 and 1000 Mbps as well as full- and half-duplex. By default the ENET interface is configured as RGMII. The second Ethernet interface is provided at the SAI1 pins. The supply voltage must be set externally to 1.8 V or 3.3 V, with LGA pads V_ENET and V_SAI1_SAI5, see also chapter 3.2.8.6.
The differential signals are length matched on the TQMa8MPxL and routed with a differential impedance of 100 Ω.
On the carrier board they have to be connected according to RGMII specifications.

The following table shows the signals used in RGMII mode.

Table 8: ENET signals in RGMII mode

Signal	Ethernet	Direction	i.MX 8M Plus	TQMa8MPxL	Power group
ENET_QOS_RX_CTL	ENET1	I	AE28	AA4	V_ENET
ENET_QOS_RXC	ENET1	I	AE29	AB7	
ENET_QOS_RD0	ENET1	I	AG29	AB4	
ENET_QOS_RD1	ENET1	I	AG28	AB5	
ENET_QOS_RD2	ENET1	I	AF29	AA6	
ENET_QOS_RD3	ENET1	I	AF28	Y7	
ENET_QOS_TX_CTL	ENET1	O	AF24	Y8	
ENET_QOS_TXC	ENET1	O	AE24	AB9	
ENET_QOS_TD0	ENET1	O	AC25	AA8	
ENET_QOS_TD1	ENET1	O	AE26	AB8	
ENET_QOS_TD2	ENET1	O	AF26	Y9	
ENET_QOS_TD3	ENET1	O	AD24	AA10	
ENET_QOS_MDC	ENET1	O	AH28	Y5	
ENET_QOS_MDIO	ENET1	I/O	AH29	Y6	
ENET_QOS_EVENT2_OUT	ENET1	O	AJ14	B8	V_SAI2_SAI3_SPDIF
ENET_QOS_EVENT2_IN	ENET1	I	AH16	B9	
ENET1_RST#	ENET1	O	AC10	L4	V_SAI1_SAI5
ENET1_INT#	ENET1	O	AF10	H4	
ENET0_RST#	ENET0	O	AJ9	K4	
ENET0_INT#	ENET0	I	AH8	G4	
ENET_MDC	ENET0	O	AH9	H3	
ENET_MDIO	ENET0	I/O	AJ8	J3	
ENET_RD0	ENET0	I	AD10	J2	
ENET_RD1	ENET0	I	AE10	K2	
ENET_RD2	ENET0	I	AH10	L3	
ENET_RD3	ENET0	I	AH12	M3	
ENET_RXC	ENET0	I	AJ12	K1	
ENET_TD0	ENET0	O	AJ11	M2	
ENET_TD1	ENET0	O	AJ10	N2	
ENET_TD2	ENET0	O	AH11	P3	
ENET_TD3	ENET0	O	AD12	R3	
ENET_TX_CTL	ENET0	O	AH13	R4	
ENET_TXC	ENET0	O	AH14	R2	
ENET_RX_CTL	ENET0	I	AF12	P4	

3.2.5.6 I²C

Four I²C interfaces provided by the i.MX 8M Plus are routed to TQMa8MPxL LGA pads.
All I²C devices on the TQMa8MPxL are controlled by the I2C1 bus.

The following table shows the signals used by the I²C interfaces.

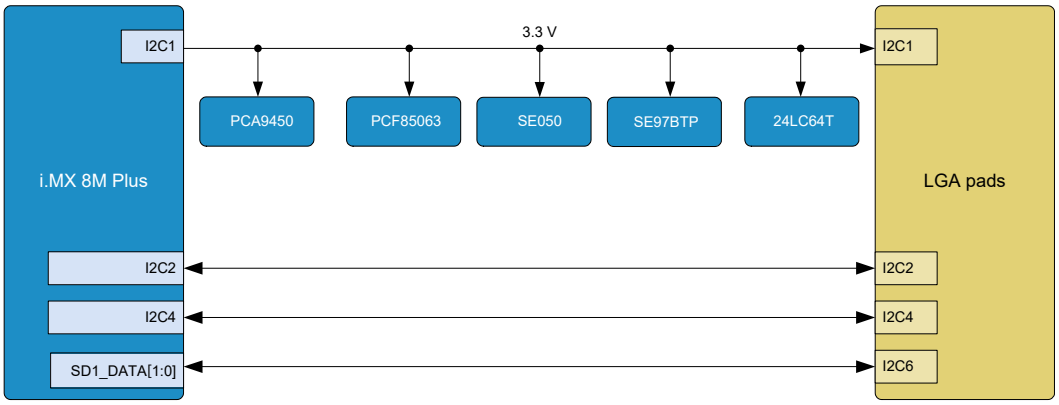


Figure 7: Block diagram I²C

Table 9: I²C signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Power group	Remark
I2C1_SCL	O	AC8	C14	3.3 V	4.7 kΩ PU to 3.3 V on TQMa8MPxL
I2C1_SDA	I/O	AH7	D13		4.7 kΩ PU to 3.3 V on TQMa8MPxL
I2C2_SCL	O	AH6	C13		No PU on TQMa8MPxL
I2C2_SDA	I/O	AE8	C12		No PU on TQMa8MPxL
I2C4_SCL	O	AF8	B14		No PU on TQMa8MPxL
I2C4_SDA	I/O	AD8	B13		No PU on TQMa8MPxL
I2C6_SCL	O	Y29	V10	V_SD1	No PU on TQMa8MPxL
I2C6_SDA	I/O	Y28	W10		No PU on TQMa8MPxL

The following table shows the I²C devices controlled by the I2C1 bus on the TQMa8MPxL.

Table 10: Address assignment I2C1 bus

Component	Function	7-bit address
PCA9450	PMIC	0x25 / 010 0101b
24LC64T	EEPROM (optional)	0x57 / 101 0111b
PCF85063A	RTC (optional)	0x51 / 101 0001b
SE97BTP	EEPROM (Normal Mode)	0x53 / 101 0011b
	EEPROM (Protection Mode)	0x33 / 011 0011b
	Temperature sensor in EEPROM	0x1B / 001 1011b
SE050	Trust Secure Element (optional)	0x48 / 100 1000b

If more devices are connected to the I2C1 bus on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. Additional pull-ups should be provided at the I²C bus on the carrier board, if required.

3.2.5.7 JTAG

The processor provides a JTAG interface that can be used to debug the programs executed on the processor. A corresponding hardware tool is required for this. The interface can also be configured for Boundary Scan.

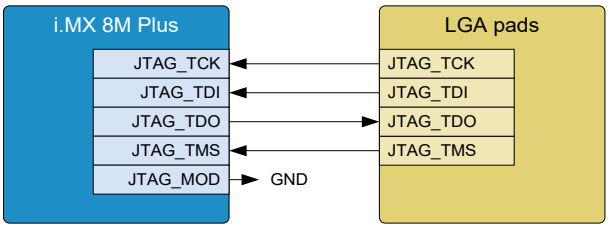


Figure 8: Block diagram JTAG interface

The following table shows the signals used by the JTAG interface. An external circuit on the mainboard has not to be provided.

Table 11: JTAG signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Remark	Power group
JTAG_TCK	I	G18	M19	–	3.3 V
JTAG_TDI	I	G16	P18	–	
JTAG_TDO	O	F14	L19	–	
JTAG_TMS	I	G14	N18	–	
JTAG_MOD	I	G20	–	10 kΩ PD on TQMa8MPxL	

3.2.5.8 GPIO

Except for the dedicated differential signals, e.g., MIPI DSI/CSI, and USB, all CPU signals routed to the TQMa8MPxL LGA pads can be configured as GPIO. The electrical characteristics of the GPIOs are to be taken from the i.MX 8M Plus Data Sheet (2).
The following table shows the GPIO signals primarily configured as GPIO.

Table 12: GPIO signals

Signal	i.MX 8M Plus	TQMa8MPxL	Power group
GPIO1_IO00	A7	E16	–
GPIO1_IO01	E8	E15	–
GPIO1_IO03	D6	E14	–
GPIO1_IO06	A3	E12	–
GPIO1_IO07	F6	E11	–
GPIO1_IO09	B8	D11	–
GPIO3_IO14	R26	C16	–
GPIO2_IO06	U26	U8	V_SD1
GPIO2_IO07	AA29	U9	
GPIO2_IO10	W25	V6	
GPIO2_IO11	W26	W7	
GPIO3_IO19	AC14	D2	V_SAI1_SAI5
GPIO3_IO20	AD14	A2	
GPIO3_IO21	AE16	C2	
GPIO4_IO18	AC12	N4	
GPIO4_IO19	AJ13	T2	
GPIO4_IO20	AE12	L1	
GPIO4_IO28	AJ19	A9	V_SAI2_SAI3_SPDIF
GPIO4_IO27	AJ15	A6	
GPIO4_IO21	AH17	B6	
GPIO4_IO22	AJ16	A7	
GPIO4_IO24	AJ17	C7	
GPIO4_IO25	AH15	C9	
GPIO4_IO29	AJ18	A10	
GPIO5_IO04	AD18	L5	
GPIO5_IO05	AC18	L6	
GPIO5_IO03	AE18	M6	
GPIO5_IO27	AJ4	E9	–
GPIO5_IO26	AE6	F9	–
GPIO5_IO07	AC20	G1	–
GPIO5_IO06	AF20	H1	–
GPIO5_IO09	AE20	F2	–
GPIO5_IO08	AD20	G2	–

3.2.5.9 MIPI CSI

The i.MX 8M Plus provides two MIPI-CSI camera interfaces with four data pairs each.
When using one camera interface, the maximum image format is 4K at 45 fps or 12MP at 30 fps.
When using both camera interfaces, up to 1080p at 80 fps is supported. The maximum bit rate is 1.5 Gbps.
The differential signals are length matched on the TQMa8MPxL and routed with a differential impedance of 100 Ω.

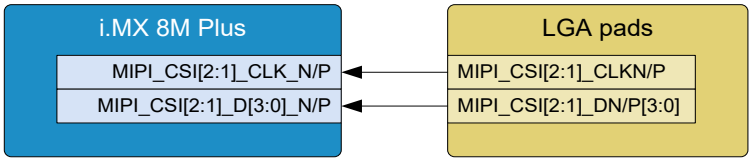


Figure 9: Block diagram MIPI CSI

The following table shows the signals used by the MIPI CSI interface.

Table 13: MIPI CSI signals

Signal	i.MX 8M Plus	TQMa8MPxL	Power group
CSI1_D1_N	E20	K20	1.8 V
CSI1_D1_P	D20	L20	
CSI1_D3_N	E26	N20	
CSI1_D3_P	D26	P20	
CSI1_CLK_N	E22	L22	
CSI1_CLK_P	D22	M22	
CSI1_D0_N	E18	J21	
CSI1_D0_P	D18	K21	
CSI1_D2_N	E24	M21	
CSI1_D2_P	D24	N21	
CSI2_D1_N	B24	R21	
CSI2_D1_P	A24	T21	
CSI2_D3_N	B21	V21	
CSI2_D3_P	A21	W21	
CSI2_CLK_N	B23	T20	
CSI2_CLK_P	A23	U20	
CSI2_D0_N	B25	P22	
CSI2_D0_P	A25	R22	
CSI2_D2_N	B22	U22	
CSI2_D2_P	A22	V22	

3.2.5.10 MIPI DSI

The i.MX 8M Plus provides a DSI interface with four data pairs to output serial display data at up to 1.5 Gbps.
The MIPI-DSI PHY supports resolutions up to 1920x1200 @ 60 fps.
The differential signals are length matched on the TQMa8MPxL and routed with a differential impedance of 100 Ω.

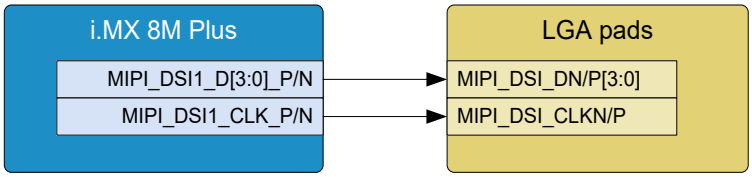


Figure 10: Block diagram MIPI DSI

The following table shows the signals used by the MIPI DSI interface.

Table 14: MIPI DSI signals

Signal	i.MX 8M Plus	TQMa8MPxL	Power group
DSI_CLK_N	B18	F21	1.8 V
DSI_CLK_P	A18	G21	
DSI_D0_N	B16	D20	
DSI_D0_P	A16	E20	
DSI_D1_N	B17	E22	
DSI_D1_P	A17	F22	
DSI_D2_N	B19	G20	
DSI_D2_P	A19	H20	
DSI_D3_N	B20	H22	
DSI_D3_P	A20	J22	

3.2.5.11 HDMI

The i.MX 8M Plus provides an HDMI interface according to the display specification "HDMI 2.0a" incl. eARC.
The maximum resolutions are 3840x2160 @ 30 fps or 1920x1080 @ 120 fps. The interface operates with 1.8 V.
The differential signals are length matched on the TQMa8MPxL and routed with a differential impedance of 100 Ω.

Table 15: HDMI signals

Signal	i.MX 8M Plus	TQMa8MPxL	Power group
EARC_AUX	AH23	V4	1.8 V
EARC_N_HPD	AH22	T1	
EARC_P_UTIL	AJ23	U1	
HDMI_CEC	AD22	W4	
HDMI_TXC_N	AJ24	U3	
HDMI_TXC_P	AH24	V3	
HDMI_DDC_SCL	AC22	AB3	
HDMI_DDC_SDA	AF22	AB2	
HDMI_HPD	AE22	Y3	
HDMI_TX0_N	AJ25	V2	
HDMI_TX0_P	AH25	W2	
HDMI_TX1_N	AJ26	W1	
HDMI_TX1_P	AH26	Y1	
HDMI_TX2_N	AJ27	Y2	
HDMI_TX2_P	AH27	AA2	

3.2.5.12 LVDS

In addition to MIPI-DSI and HDMI, the CPU provides an LVDS interface. The CPU only offers one PHY, but supports up to two channels with up to four data lanes each. The maximum resolution is 1920 x 1200 at 60 fps. The interface operates with 1.8 V. The differential signals are length matched on the TQMa8MPxL and routed with a differential impedance of 100 Ω.

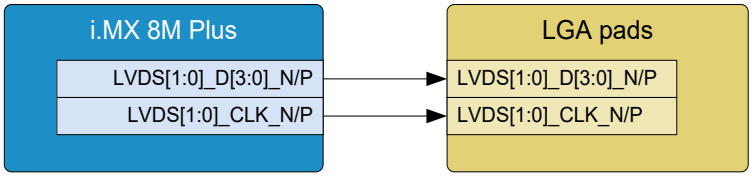


Figure 11: Block diagram LVDS

Table 16: LVDS signals

Signal	i.MX 8M Plus	TQMa8MPxL	Power group
LVDS0_D0_N	E28	Y10	1.8 V
LVDS0_D0_P	D29	Y11	
LVDS0_D1_N	F28	AA11	
LVDS0_D1_P	E29	AA12	
LVDS0_D2_N	H28	AB12	
LVDS0_D2_P	G29	AB13	
LVDS0_D3_N	J28	AA14	
LVDS0_D3_P	H29	AA15	
LVDS0_CLK_N	G28	Y13	
LVDS0_CLK_P	F29	Y14	
LVDS1_D0_N	B26	AB15	
LVDS1_D0_P	A26	AB16	
LVDS1_D1_N	B27	Y16	
LVDS1_D1_P	A27	Y17	
LVDS1_D2_N	C28	AA17	
LVDS1_D2_P	B29	AA18	
LVDS1_D3_N	D28	AA19	
LVDS1_D3_P	C29	AA20	
LVDS1_CLK_N	B28	AB18	
LVDS1_CLK_P	A28	AB19	

3.2.5.13 PCIe

The i.MX 8M Plus provides a PCIe Gen3 interface with one (x1) lane.

The 100 MHz reference clock can be generated on the TQMa8MPxL and output to PCIE_REF_CLKN/P for the PCIe card.

Alternatively, the reference clock can be provided from an external source to PCIE_REF_CLKN/P. In general, NXP recommends the use of an external source for accuracy reasons.

The series capacitors required by the PCIe standard must be provided on the carrier board.

The differential signals are length matched on the TQMa8MPxL and routed with a differential impedance of 85 Ω.

The signals must be terminated on the carrier board according to the PCIe specification.

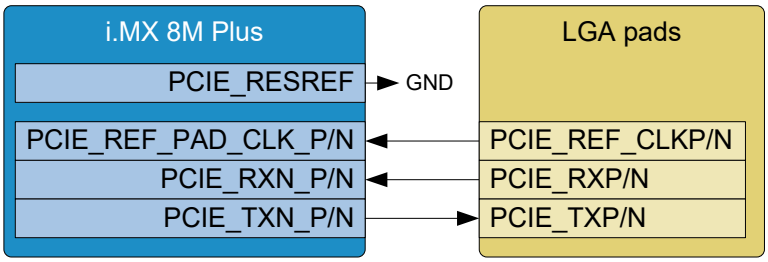


Figure 12: Block diagram PCIe

Table 17: PCIe signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Power group
PCIE_REF_CLKN	I/O	E16	Y22	1.8 V
PCIE_REF_CLKP		D16	AA22	
PCIE_RXN	I	B14	W20	
PCIE_RXP		A14	Y20	
PCIE_TXN	O	B15	AA21	
PCIE_TXP		A15	AB21	
PCIE_RESREF	I	F16	–	8.2 kΩ PD on TQMa8MPxL

Attention: Accelerated aging of PCI Express PHY	
	Due to an erratum of the i.MX 8M Plus the PCI Express PHY is subject to accelerated aging in lower power states. In the i.MX 8M Plus errata (5), NXP describes a workaround that must be followed to avoid the aging impact to the PCI Express PHY.

3.2.5.14 SAI

The i.MX 8M Plus provides several SAI interfaces with different bus widths. The 8-bit SAI1 is not available since it is multiplexed as Ethernet interface. Modules from Rev.02xx use only the SAI3 interface. The supply voltage has to be set to 1.8 V or 3.3 V on the carrier board with LGA pad V_SAI2_SAI3_SPDIF. Clock pins can be used as input or output.

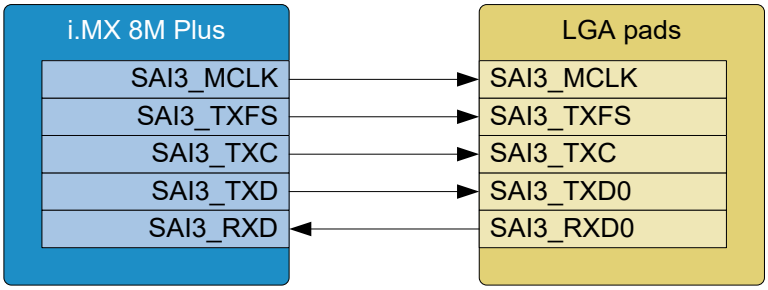


Figure 13: Block diagram SAI1

The following table lists all SAI signals provided by the TQMa8MPxL:

Table 18: SAI signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Power group
SAI3_TXFS	O	AC16	B11	V_SAI2_SAI3_SPDIF
SAI4_RXD	I	AF18	A12	
SAI3_TXc	O	AH19	B12	
SAI3_TXD	O	AH18	A13	
SAI3_MCLK	O	AJ20	C10	

3.2.5.15 SPDIF

The i.MX 8M Plus has an SPDIF interface that is not used natively. Instead, the pins are multiplexed as GPIOs by default. This configuration can be changed if necessary, for example using the LGA pads shown in the following figure:

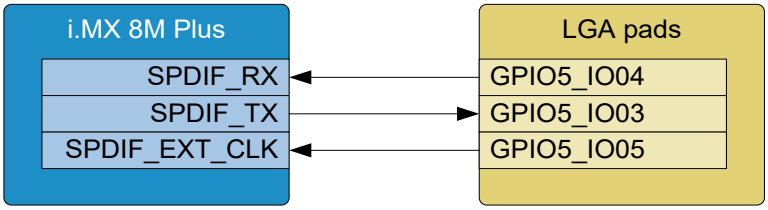


Figure 14: Block diagram SPDIF

3.2.5.16 QSPI / NAND

The NOR flash signals are routed to the TQMa8MPxL LGA pads. The NOR flash signals use a part of the NAND pins of the i.MX 8M Plus. All other NAND pins of the i.MX 8M Plus are used TQMa8MPxL-internally for the eMMC as uSDHC3 boot source. These LGA pads cannot be used if the QSPI NOR flash is equipped! For more information regarding QSPI see chapter 3.2.2.3.

Table 19: QSPI signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Power group
QSPI_A_DATA3	I/O	N24	W12	1.8 V
QSPI_A_DATA2	I/O	L24	W13	
QSPI_A_DATA1	I/O	L25	V13	
QSPI_A_DATA0	I/O	R25	V14	
QSPI_A_SS0#	O	L26	V15	
QSPI_A_SCLK	O	N25	W15	

3.2.5.17 ECSPI

The full-duplex SPI interfaces of the i.MX 8M Plus support both master and slave modes with data rates of up to 52 Mbit/s. All SPI interfaces provide one chip select each and are directly routed to the TQMa8MPxL LGA pads.
ECSPI2 is supplied with 1.8 V. ECSPI3, which is multiplexed with the UART signals, is supplied with 3.3 V.

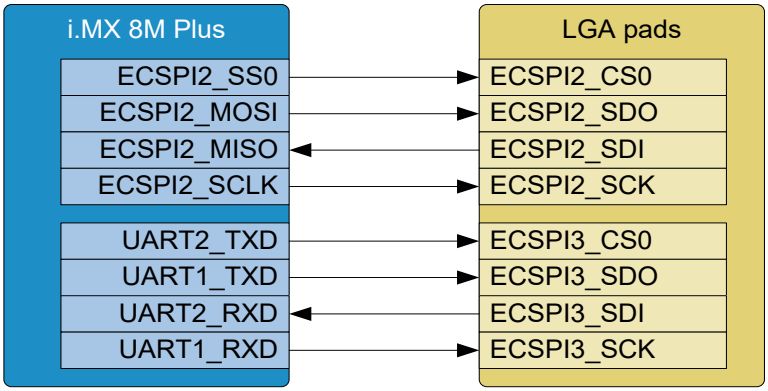


Figure 15: Block diagram ECSPI

The following table shows the signals used by the ECSPI interface.

Table 20: ECSPI signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Power group
ECSPI2_MOSI	O	AJ21	P5	1.8 V
ECSPI2_MISO	I	AH20	N5	
ECSPI2_SCLK	O	AH21	M5	
ECSPI2_SS0	O	AJ22	P6	
ECSPI3_MOSI	O	AJ3	J6	3.3 V
ECSPI3_MISO	I	AF6	J5	
ECSPI3_SCLK	O	AD6	K5	
ECSPI3_SS0	O	AH4	H5	

3.2.5.18 UART

The i.MX 8M Plus provides four UART interfaces, which are all routed to TQMa8MPxL LGA pads.
The voltage supply for UART1, UART2 and UART3 must be externally set to 1.8 V or 3.3 V via LGA pad Y19, V_SD1.
UART4 is fixed supplied with 3.3 V.

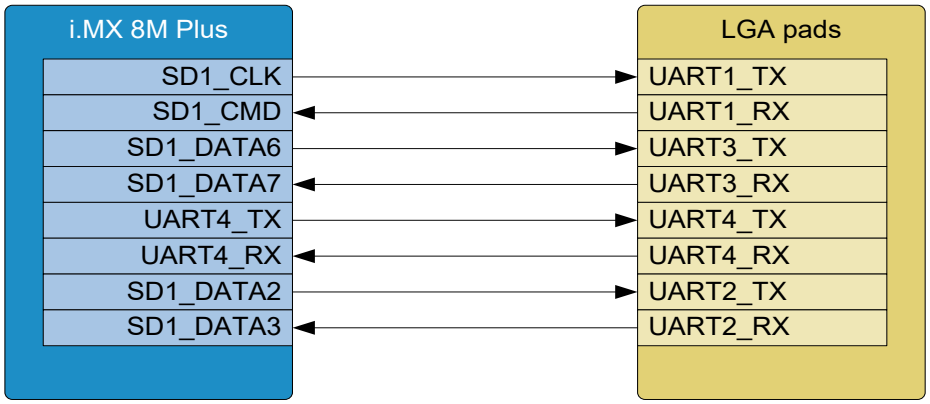


Figure 16: Block diagram UART interfaces

The following table shows the signals used by the UART interfaces.

Table 21: UART signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Power group
UART1_TXD	O	W28	V11	V_SD1
UART1_RXD	I	W29	V12	
UART2_TXD	O	V29	V9	
UART2_RXD	I	V28	W9	
UART3_TXD	O	AA28	V7	
UART3_RXD	I	U25	V8	
UART4_TXD	O	AH5	G6	3.3 V
UART4_RXD	I	AJ5	H6	

3.2.5.19 USB

The i.MX 8M Plus provides two USB 3.0 interfaces with integrated PHYs via USB1 and USB2. These support Super-Speed (5 Gbit/s), High-Speed (480 Mbit/s), Full-Speed (12 Mbit/s), as well as Low-Speed (1.5 Mbit/s) and offer host, device and OTG 2.0 functionalities. The OTG signals are provided via GPIO1 pins.

All signals have 3.3 V level. Up to 5 V can be applied to the VBUS pins. The 30 kΩ resistors required by NXP are already provided on the module.

The differential signals are length matched on the TQMa8MPxL and routed with a differential impedance of 90 Ω.

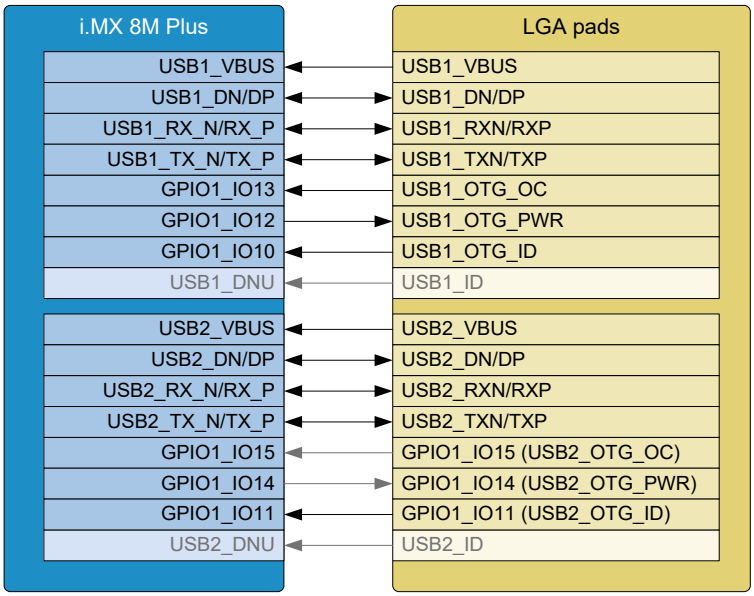


Figure 17: Block diagram USB interfaces

Table 22: USB signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Power group	Note
USB1_VBUS	P	A11	F18	5 V tolerant	
USB1_OTG_OC	I	A6	H19	3.3 V	
USB1_OTG_PWR	O	A5	H18		
USB1_OTG_ID	I	B7	G18		
USB1_ID	I	B11	F19		NXP: Do not use
USB1_DN	I/O	E10	C22		
USB1_DP	I/O	D10	B22		
USB1_RXN	I	B9	B20		
USB1_RXP	I	A9	B19		
USB1_TXN	O	B10	A21		
USB1_TXP	O	A10	A20		
USB2_VBUS	P	D12	E17	5 V tolerant	
USB2_OTG_OC	I	B5	D18	3.3 V	Multiplexed as GPIO1_IO15
USB2_OTG_PWR	O	A4	D17		Multiplexed as GPIO1_IO14
USB2_OTG_ID	I	D8	E19		Multiplexed as GPIO1_IO11
USB2_ID	I	E12	D19		NXP: Do not use
USB2_DN	I/O	E14	C19		
USB2_DP	I/O	D14	C18		
USB2_RXN	I	B12	B17		
USB2_RXP	I	A12	B16		
USB2_TXN	O	B13	A18		
USB2_TXP	O	A13	A17		

3.2.5.20 uSDHC

The i.MX 8M Plus provides three uSDHC interfaces: uSDHC1, uSDHC2 and uSDHC3. uSDHC1 is configured as UART and I2C, see chapters 3.2.5.18 and 3.2.5.6. All three interfaces support the SD standard up to version 3.0, the MMC standard up to version 5.1, and 1.8 V and 3.3 V operation. uSDHC1 and uSDHC3 provide 8-bit wide interfaces, uSDHC2 provides a 4-bit wide interface.

uSDHC1

The voltage level of uSDHC1 can be set to 1.8 V or 3.3 V by TQMa8MPxL LGA pad V_SD1, Y19. Since all essential i.MX 8M Plus signals are routed to TQMa8MPxL LGA pads, an eMMC can be connected on the carrier board. In this case the supply voltage must be set to 1.8 V. Booting from uSDHC1 is only possible after burning boot fuses and is therefore not supported by default.

uSDHC2

An SD card can be connected to the uSDHC2 interface. All i.MX 8M Plus signals required are routed to TQMa8MPxL LGA pads. SD2_VSELECT (GPIO1_IO04) is used to control the SD card supply voltage and is not routed to a TQMa8MPxL LGA pad. The signal SD2_RESET_B can be ignored if the SD card is supplied by the TQMa8MPxL. The voltage V_SD2 is provided for external pull-ups.

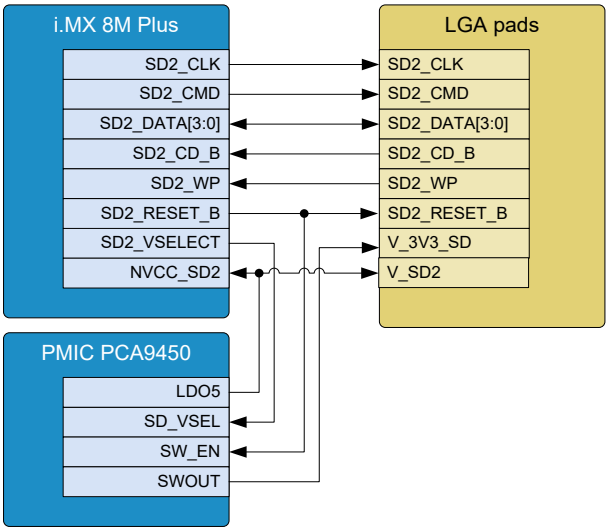


Figure 18: Block diagram SD card interface

Table 23: USDHC2 signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Power group
SD2_DATA3	I/O	AA25	T5	SD2_VSELECT
SD2_DATA2	I/O	AA26	U5	
SD2_DATA1	I/O	AC29	V5	
SD2_DATA0	I/O	AC28	W5	
SD2_CLK	O	AB29	T4	
SD2_CD#	I	AD29	R6	
SD2_CMD	I/O	AB28	U6	
SD2_WP	I	AC26	T7	
SD2_RST# [3]	O	AD28	U7	

uSDHC3

The uSDHC3 interface uses a part of the NAND pins, on the TQMa8MPxL the eMMC is connected to it.

3: 4.7 kΩ PU on TQMa8MPxL.

3.2.5.21 External clock sources

The i.MX 8M Plus has the option to use two external oscillators as clock sources.
All four i.MX 8M Plus signals provided for this purpose are routed to TQMa8MPxL LGA pads.
The following table shows these clock signals.

Table 24: CLK signals

Signal	i.MX 8M Plus	TQMa8MPxL	Power group
CLK1_IN	K28	W18	1.8 V
CLK2_IN	L28	W16	
CLK1_OUT	K29	W17	
CLK2_OUT	L29	V17	

3.2.6 Unspecific signals

The following table lists all signals that are not assigned to a specific group.
ISO_7816 and ISO_14443 signals are only available with assembled Trust Secure Element, see chapter 3.2.3.

Table 25: Unspecific signals

Signal	Direction	i.MX 8M Plus	TQMa8MPxL	Remark
PMIC_WDOG_OUT#	O	B6	F8	3.3 V
PMIC_WDOG_IN#	I	–	F6	3.3 V, 100 kΩ PU on TQMa8MPxL
M7_NMI	I	B4	V19	3.3 V active high
TEMP_EVENT#	O_{OD}	–	U19	0.9 V to 3.6 V
RTC_EVENT#	O_{OD}	–	U18	0.7 V to 5.5 V
ISO_7816_CLK	I	–	J19	Use with populated Trust Secure Element
ISO_7816_RST	I	–	L18	
ISO_7816_IO1	I/O	–	K18	
ISO_7816_IO2	I/O	–	J18	
ISO_14443_LA	I/O	–	D21	
ISO_14443_LB	I/O	–	C21	

3.2.7 Reset

Reset inputs or outputs are available at the TQMa8MPxL LGA pads.
The following block diagram shows the wiring of the reset signals.

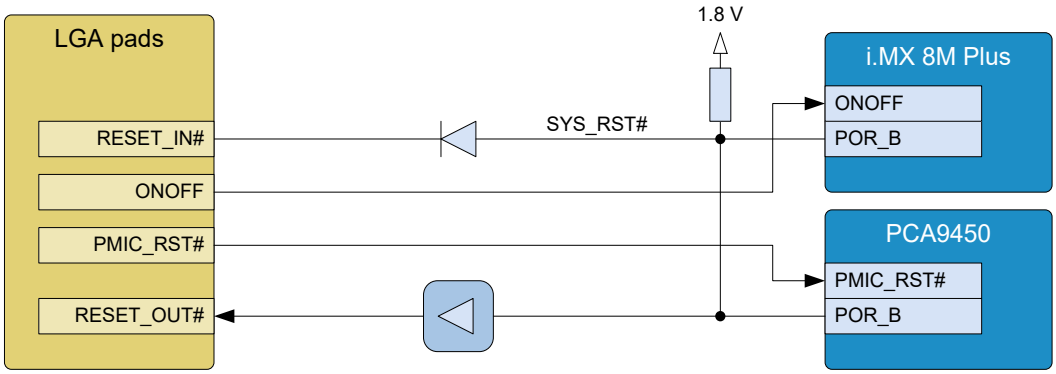


Figure 19: Block diagram Reset

The following table describes the reset signals available at the TQMa8MPxL LGA pads:

Table 26: Reset signals

Signal	Direction	TQMa8MPxL	Power group	Remark
RESET_IN#	I	E7	3.3 V	• Activates RESET (POR_B) of the i.MX 8M Plus; low-active. • External pull-up to 3.3 V required. • Pull to GND to activate.
RESET_OUT#	O	F7	–	• Open drain output; low-active. • Activates RESET of carrier board components. • External pull-up required (max. 5.5 V).
PMIC_RST#	I	E6	1.8 V	• No pull-up on carrier board required; low-active. • Programmable PMIC response (warm reset, cold reset).
ONOFF	I	G7	1.8 V	• ON/OFF function of the i.MX 8M Plus (see CPU data sheet (2)). • No pull-up on carrier board required; low-active. • Pull to GND for 5 s to activate.

3.2.8 Power

3.2.8.1 Power supply

The TQMa8MPxL requires a supply voltage of 5 V ±5 %. The characteristics and functions of a certain pin or signal is to be taken from the PMIC Data Sheet (4), and the i.MX 8M Plus Data Sheet (2).

3.2.8.2 Power consumption

The given power consumption has to be seen as an approximate value.
The TQMa8MPxL power consumption strongly depends on the application, the mode of operation and the operating system.
For more information on power consumption and savings options, see NXP Application Note AN12410 (6).

The following table shows TQMa8MPxL (with i.MX 8M Plus Quad) power supply (V_5V_IN) and power consumption parameters:

Table 27: Power consumption

Mode of operation	Current @ 5 V	Power consumption @ 5 V
Theoretical calculated peak (worst case)	3.625 A	18.1 W
U-Boot prompt	0.36 A	1.8 W
Linux-Idle	341.7 mA	1.7 W
Linux with 100 % CPU load	716.1 mA	3.6 W
Reset	0.140 mA	0.7 mW
Suspend to RAM mode	25.60 mA	128 mW

3.2.8.3 Voltage monitoring

The TQMa8MPxL features a supervisor which monitors the input voltage (V_{IN}).
If the input voltage drops below 4.38 V, a Reset is triggered and the TQMa8MPxL is held in reset until the input voltage is in the permitted range again.

Attention: Destruction or malfunction, supply voltage exceedance	
	The voltage monitoring does not detect an exceedance of the permitted input voltage. An exceedance of the permitted input voltage may cause malfunction, destruction or accelerated ageing of the TQMa8MPxL.

3.2.8.4 Other supply voltages

USBx_VBUS:

The voltage inputs USB1_VBUS and USB2_VBUS are used to detect the USB-VBUS voltage and are usually connected to the VBUS voltage switched by USB[2:1]_PWR. Protective circuitry on the TQMa8MPxL permits up to 5 V to be applied to these LGA pads.
It is recommended to provide one 220 nF capacitor (10 V) each between USBx_VBUS and Ground on the carrier board.

V_LICELL:

A coin cell can be connected to the TQMa8MPxL LGA pad D15, V_LICELL, to supply the optional discrete RTC.
See chapter 3.2.4.2 for information on the LICELL or RTC options.

Note: RTC power supply	
	If a discrete RTC is supplied by a coin cell, the CPU-internal RTC is not reset in case of a supply voltage failure.

3.2.8.5 Supply outputs

The TQMa8MPxL provides three voltages that can be used on the carrier board.

Table 28: Voltages provided by TQMa8MPxL

Voltage	TQMa8MPxL	Usage	Max. load
V_1V8	N1	General usage on carrier board	500 mA
V_3V3	P1	General usage on carrier board	500 mA
V_3V3_SD	G5	SD card supply	400 mA

The voltage V_3V3 can be used as Power-Good signal for the supply of circuitry on the carrier board.

Attention: Destruction or malfunction, current exceedance	
	A load of up to 500 mA at V_1V8 or V_3V3, as well as up to 400 mA at V_3V3_SD causes an increased power consumption of the TQMa8MPxL and thus a higher self-heating. These three voltages are outputs and must never be supplied from external sources! Furthermore the outputs are not short-circuit proof. Overloading the voltage outputs can damage the TQMa8MPxL.

3.2.8.6 Configurable voltages

The TQMa8MPxL provides four LGA pads that define the I/O voltages for specific rails of the CPU. These are listed in the following table and must be defined on the carrier board. If not defined, the corresponding I/O signals are not supplied with voltage. For this purpose the outgoing voltages V_1V8 or V_3V3 can be used.

Table 29: Configurable voltages

Signal	TQMa8MPxL	Permitted voltages	Remark
V_ENET	AB10	1.8 V or 3.3 V	RGMII: 1.8 V RMII: 1.8 V or 3.3 V
V_SAI1_SAI5	B15	1.8 V or 3.3 V	–
V_SAI2_SAI3_SPDIF	A15	1.8 V or 3.3 V	–
V_SD1	Y19	1.8 V or 3.3 V	–

3.2.8.7 Power-Up sequence TQMa8MPxL / carrier board

Since the TQMa8MPxL operates with 5 V and the I/O voltages of the CPU signals are generated on the TQMa8MPxL, there are timing requirements for the carrier board design with respect to the voltages generated on the carrier board:

After power up of the 5V supply for the TQMa8MPxL, the PMIC power-up sequence starts. External TQMa8MPxL inputs driven by the carrier board may only be switched on after the power-up of V_3V3. LGA pad P1 (V_3V3) can be used as feedback.

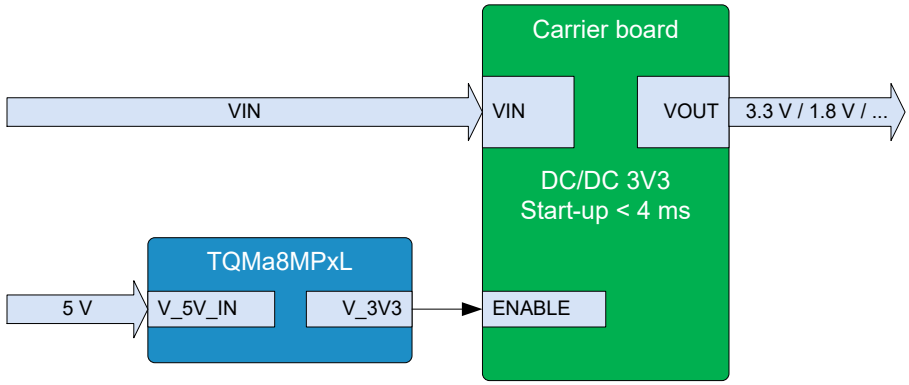


Figure 20: Block diagram power supply carrier board

Attention: Destruction or malfunction, Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the power-up sequence is indicated by a high level of signal V_3V3, LGA pad P1.

3.2.8.8 Standby and SNVS

In standby mode, several voltage controllers on the TQMa8MPxL are switched off.

The rails V_1V8_SNVS and V_0V8_SNVS remain active, which ensures the correct function of the RTC.

3.2.8.9 PMIC

The characteristics and functions of all pins and signals have to be taken from the i.MX 8M Plus Reference Manual (1) and the PMIC Data Sheet (4). The PMIC is controlled by the I2C1 bus.

- The PMIC has I²C address `0x25 / 010 0101b`

The following PMIC and power management signals are available on the TQMa8MPxL LGA pads

Table 30: PMIC signals

Signal	Direction	TQMa8MPxL	Power group	Remark
PMIC_WDOG_IN#	I_{PU}	F6	V_3V3	• Low-ctive PMIC Reset input • Triggers Cold Reset • Deactivated by default
PMIC_RST#	I	E6	V_1V8_SNVS	• Low-active PMIC Rest input with internal PU • Triggers Cold Reset by default
RESET_OUT#	O_{OD}	F7	1.8 V	• Low-active output • Connected to PMIC POR# • Can signal a TQMa8MPxL reset
SD_VSEL	–	–	–	• See chapter 3.2.5.20

Attention: Destruction or malfunction, PMIC programming	
	Improper programming of the PMIC may result in the i.MX 8M Plus or periphery being operated outside its specification. This may lead to malfunctions, accelerated aging or destruction of the TQMa8MPxL.

3.2.9 Impedances

By default, all single-ended signals have a nominal impedance of 50 Ω ±10 %.
However, some interfaces on the TQMa8MPxL are routed with different impedances, depending on the signal requirements.

The following table is taken from the Hardware Developer's Guide (3) and shows the respective interfaces:

Table 31: Impedances

Signal / Interface	Impedance on TQMa8MPxL	Recommendation for carrier board
DDR DQS/CLK; PCIe CLK, TX/RX data pairs	85 Ω, differential	85 Ω ±10 %, differential
Differential USB signals	90 Ω, differential	90 Ω ±10 %, differential
Differential MIPI (CSI, DSI), HDMI, EARC, LVDS signals	100 Ω, differential	100 Ω ±10 %, differential
Differential RGMII signals	100 Ω, differential	100 Ω ±10 %, differential

4. SOFTWARE

The TQMa8MPxL is delivered with a preinstalled boot loader U-Boot.
The BSP provided by TQ-Systems GmbH is configured for the combination of TQMa8MPxL and MBa8MPxL.
The boot loader U-Boot provides TQMa8MPxL-specific as well as board-specific settings, e.g.:

- i.MX 8M Plus configuration
- PMIC configuration
- SDRAM configuration
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

Further information can be found in the https://support.tq-group.com/TQMa8MPxL.

If another bootloader is used, this data must be adapted. Contact TQ-Support for detailed information.

5. MECHANICS

5.1 Dimensions

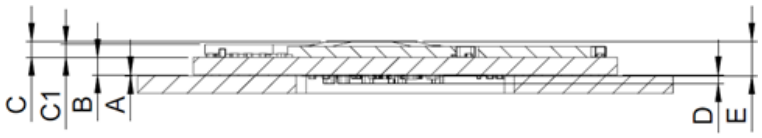


Figure 21: TQMa8MPxL dimensions, side view

Table 32: TQMa8MPxL heights

Dim.	Value	Tolerance	Remark
A	0.125 mm	+0.075 mm –0.025 mm	TQMa8MPxL LGA pads height
B	1.6 mm	±0.16 mm	PCB without solder resist
C	1.43 mm	±0.16 mm	Height CPU
C1	1.17 mm	±0.1 mm	Height of eMMC and NOR flash
D	0.57 mm	±0.2 mm	Highest component, bottom side
E	3.18 mm	±0.23 mm	Top edge CPU above carrier board, with soldered TQMa8MPxL

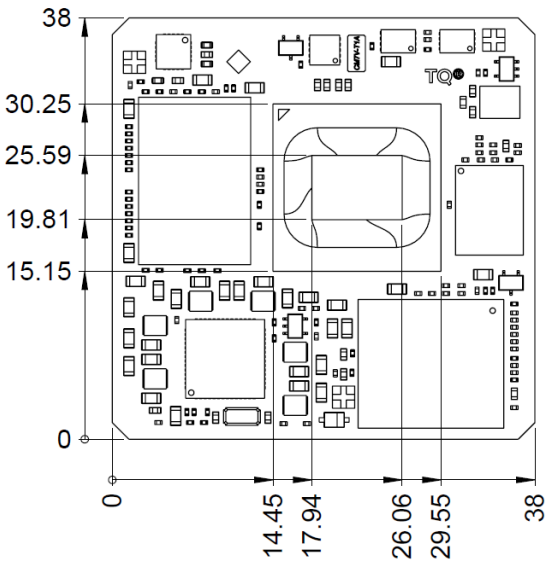


Figure 22: TQMa8MPxL dimensions, top view

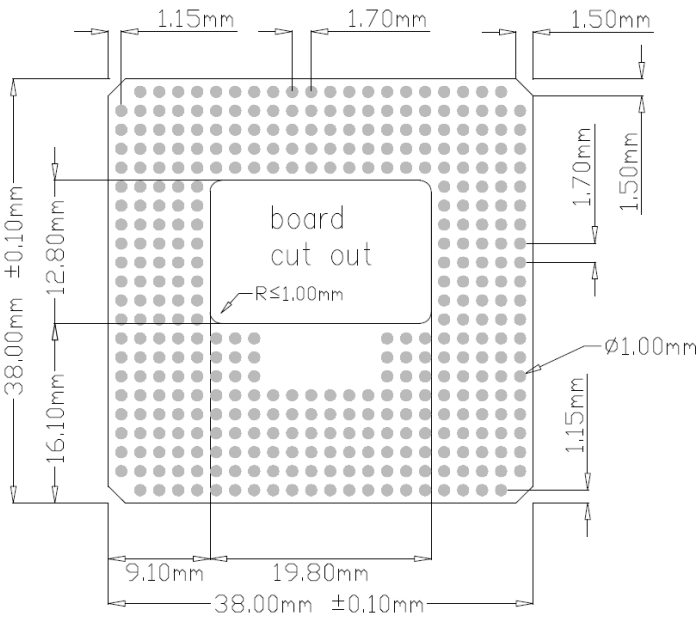


Figure 23: TQMa8MPxL dimensions, top through view

5.2 Component placement

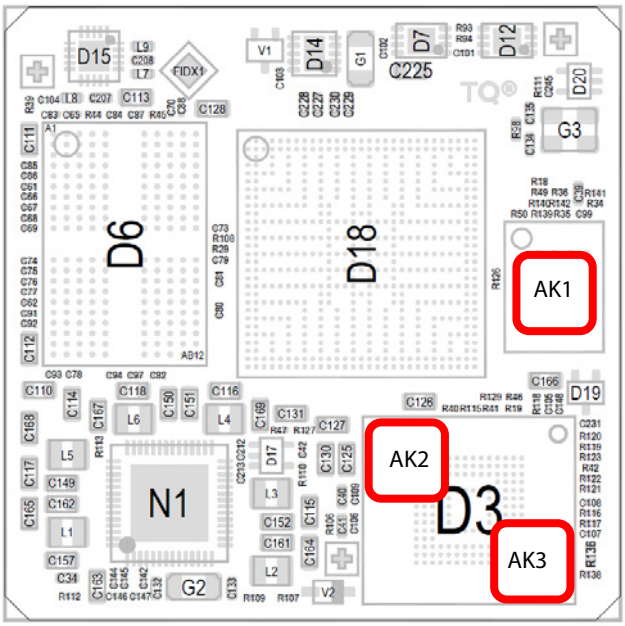


Figure 24: TQMa8MPxL, component placement top

The labels on the TQMa8MPxL show the following information:

Table 33: Labels on TQMa8MPxL

Label	Content
AK1 (on D2)	TQMa8MPxL version and revision
AK2	Serial number
AK3	MAC address

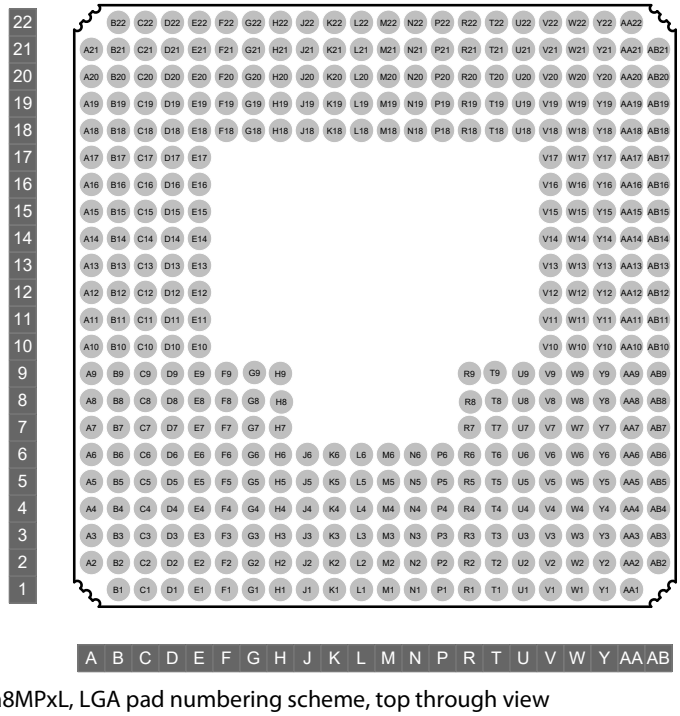


Figure 25: TQMa8MPxL, LGA pad numbering scheme, top through view

5.3 Adaptation to the environment

The TQMa8MPxL has overall dimensions (length × width) of 38 mm × 38 mm (± 0,1 mm).
The TQMa8MPxL has a maximum height above the carrier board of approximately 3.18 mm.
The TQMa8MPxL has 366 LGA pads with a diameter of 1.0 mm and a grid of 1.7 mm.
The TQMa8MPxL weighs approximately 10 g.

5.4 Protection against external effects

The TQMa8MPxL does not provide protection against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.5 Thermal management

To cool the TQMa8MPxL, noteTable 28. The power dissipation originates primarily in the i.MX 8M Plus, the LPDDR4 SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See NXP documents (6) and (7) for further information.

Attention: Destruction or malfunction, TQMa8MPxL cooling	
	The i.MX 8M Plus belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8M Plus must be taken into consideration when connecting the heat sink, see (6). The i.MX 8M Plus is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8MPxL and thus malfunction, deterioration or destruction.

5.6 Structural requirements

The TQMa8MPxL has to be soldered on the carrier board. To ensure a high-quality connection of the LGA pads during reflow soldering of the TQMa8MPxL, the LGA pads must be free of grease and dirt.
Please contact TQ-Support for soldering instructions (11).

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa8MPxL was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa8MPxL.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diode(s)
- Slow signals: RC filtering, Zener diode(s)
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Shock and Vibration

Table 34: Shock resistance

Parameter	Details
Shock	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	10 ms
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 35: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 ~ 9 Hz, 9 ~ 200 Hz, 200 ~ 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X– Y – Z axis
Acceleration	2 Hz to 9 Hz: 3.5 m/s^2 9 Hz to 200 Hz: 10 m/s^2 200 Hz to 500 Hz: 15 m/s^2

6.4 Climate and operational conditions

The TQMa8MPxL is available in three different variants (Consumer, Extended and Industrial) with different ambient temperature ranges. The operating temperature range for the TQMa8MPxL strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa8MPxL.

In general, a reliable operation is given when following conditions are met:

Table 36: Climate and operational conditions

Parameter		Range	Remark
Ambient temperature TQMa8MPxL	Consumer	0 °C to +85 °C	–
	Extended	–25 °C to +85 °C	–
	Industrial	–40 °C to +85 °C	–
T_J temperature i.MX 8M Plus		–40 °C to +105 °C	–
T_J temperature PMIC		–40 °C to +125 °C	–
Case temperature LPDDR4		–40 °C to +95 °C	–
Case temperature other ICs	Consumer	0 °C to +85 °C	–
	Extended	–25 °C to +85 °C	–
	Industrial	–40 °C to +85 °C	–
Storage temperature TQMa8MPxL		–40 °C to +85 °C	–
Relative humidity (operating / storage)		10 % to 90 %	Not condensing

Detailed information concerning the i.MX 8M Plus thermal characteristics is to be taken from NXP documents (6) and (7).

Attention: Destruction or malfunction, TQMa8MPxL cooling	
	The i.MX 8M Plus belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8M Plus must be taken into consideration when connecting the heat sink, see (6). The i.MX 8M Plus is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8MPxL and thus malfunction, deterioration or destruction.

6.5 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa95xxSA is only a sub-component of an overall system.

6.6 Intended Use

TQ DEVICES, PRODUCTS AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION IN NUCLEAR FACILITIES, AIRCRAFT OR OTHER TRANSPORTATION NAVIGATION OR COMMUNICATION SYSTEMS, AIR TRAFFIC CONTROL SYSTEMS, LIFE SUPPORT MACHINES, WEAPONS SYSTEMS, OR ANY OTHER EQUIPMENT OR APPLICATION REQUIRING FAIL-SAFE PERFORMANCE OR IN WHICH THE FAILURE OF TQ PRODUCTS COULD LEAD TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE. (COLLECTIVELY, "HIGH RISK APPLICATIONS")

You understand and agree that your use of TQ products or devices as a component in your applications are solely at your own risk. To minimize the risks associated with your products, devices and applications, you should take appropriate operational and design related protective measures.

You are solely responsible for complying with all legal, regulatory, safety and security requirements relating to your products. You are responsible for ensuring that your systems (and any TQ hardware or software components incorporated into your systems or products) comply with all applicable requirements. Unless otherwise explicitly stated in our product related documentation, TQ devices are not designed with fault tolerance capabilities or features and therefore cannot be considered as being designed, manufactured or otherwise set up to be compliant for any implementation or resale as a device in high risk applications. All application and safety information in this document (including application descriptions, suggested safety precautions, recommended TQ products or any other materials) is for reference only. Only trained personnel in a suitable work area are permitted to handle and operate TQ products and devices. Please follow the general IT security guidelines applicable to the country or location in which you intend to use the equipment.

6.7 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.8 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

6.9 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.10 Reliability and service life

The MTBF calculated for the TQMa8MPxL is 1,192,246 hours with a constant error rate @ +40 °C, Ground Benign.

The TQMa8MPxL is designed to be insensitive to shock and vibration.

The TQMa8MPxL must be assembled in accordance with the processing instructions provided by TQ-Systems GmbH.

Detailed information concerning the i.MX 8M Plus service life under different operational conditions is to be taken from the NXP Application Note (7).

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa8MPxL is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa8MPxL was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

7.5 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMa8MPxL always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMa8MPxL on account of available Standby or Sleep-Modes of the components on the TQMa8MPxL.

7.6 Battery

No batteries are assembled on the TQMa8MPxL.

7.7 Packaging

The TQMa8MPxL is delivered in reusable packaging.

7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa8MPxL, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa8MPxL is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))

- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 37: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CAN-FD	CAN with Flexible Data-Rate
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
DDR	Double Data Rate
DIN	Deutsche Industrienorm (German industry standard)
DNC	Do Not Connect
DSI	Display Serial Interface
EARC	Enhanced Audio Return Channel
ECSPI	Enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
Gbps	Gigabit per second
GPIO	General Purpose Input/Output
GPT	General-Purpose Timer
HDMI	High-Definition Multimedia Interface
I	Input
I/O	Input/Output
I2C	Inter-Integrated Circuit
IP00	Ingress Protection 00
IPU	Input with Pull-Up
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LGA	Land Grid Array
LPDDR4	Low Power DDR4
LVDS	Low-Voltage Differential Signaling
MAC	Media Access Control
MIPI	Mobile Industry Processor Interface
ML/AI	Machine Learning / Artificial Intelligence
MMC	Multimedia Card
MTBF	Mean operating Time Between Failures

8.1 Acronyms and definitions (continued)

Table 37: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NOR	Not-Or
O	Output
OD	Open Drain
OOD	Output with Open Drain
OTG	On-The-Go
P	Power
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up (resistor)
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protection
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SNVS	Secure Non-Volatile Storage
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
TBD	To Be Determined
TSE	Trust Secure Element
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 38: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 8M Plus Applications Processor Reference Manual	Rev. 1, Jun 2021	NXP
(2)	i.MX 8M Plus Applications Processors Data Sheet	Rev 1, Aug 2021	NXP
(3)	i.MX 8M Plus Hardware Developer's Guide	Rev 0, Mar 2021	NXP
(4)	PMIC PCA9450 Data Sheet	Rev 2.2, Sep 2021	NXP
(5)	i.MX 8M Plus Mask Set Errata for Mask P33A	Rev. 2, Oct 2021	NXP
(6)	i.MX 8M Plus Power Consumption Measurement, AN12410	Rev. 0, 14 Apr 2019	NXP
(7)	i.MX 8M Plus Product Lifetime Usage, AN12468	Rev.0, 23 Jun 2019	NXP
(8)	SE050 Trust Secure Element Data Sheet	Rev. 3.1, Dec 2020	NXP
(9)	MBa8MPxL User's Manual	– current –	TQ-Systems
(10)	TQMa8MPxL Support-Wiki	– current –	TQ-Systems
(11)	TQMa8MPxL Processing instructions	– current –	TQ-Systems

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