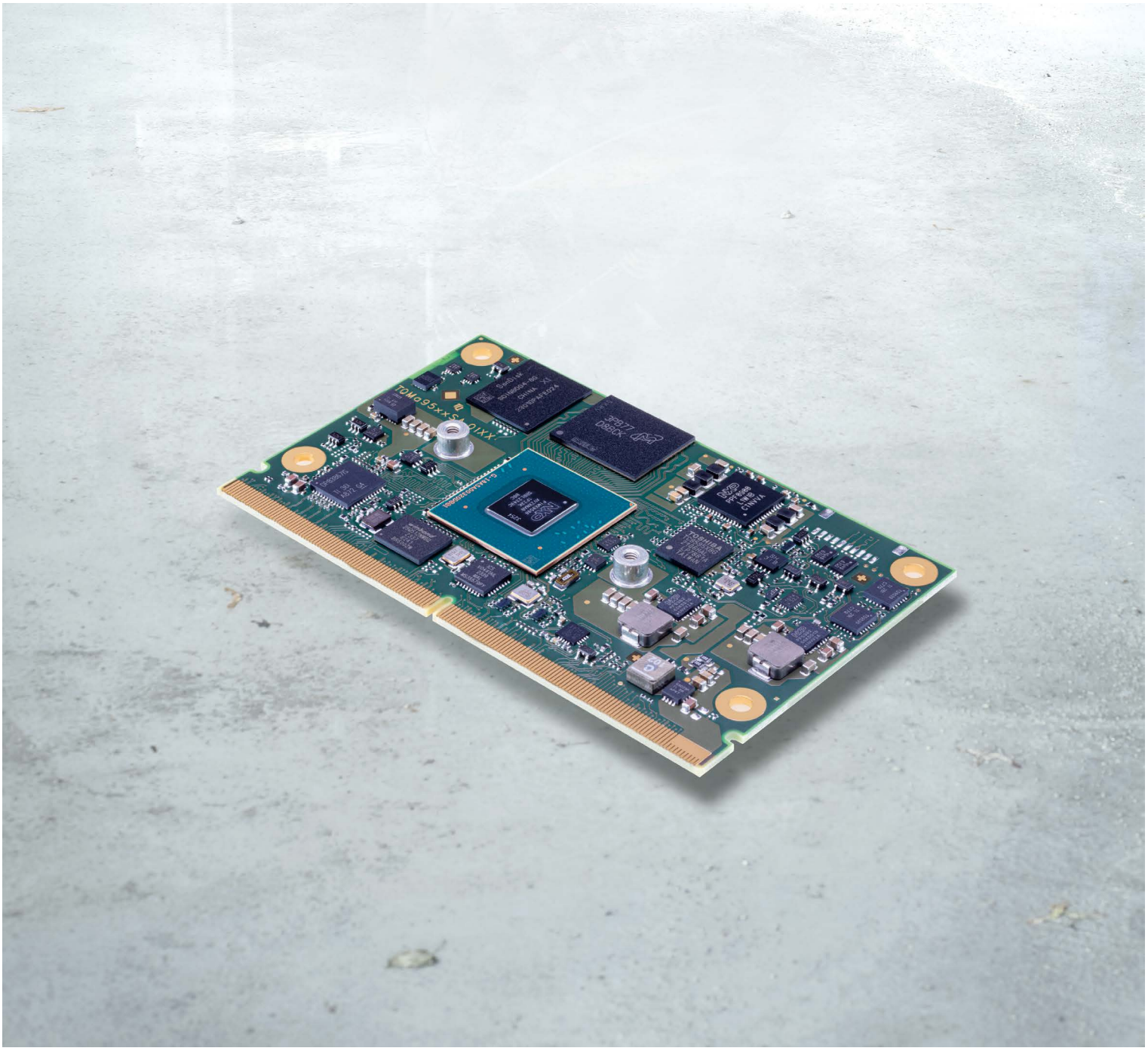
TQMa95xxSA
Preliminary User's Manual

TQMa95xxSA UM 0001
21.10.2024



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REVISION HISTORY

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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa95xxSA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MB-SMARC-2 circuit diagram
- MB-SMARC-2 User's Manual
- i.MX 95 Data Sheet
- i.MX 95 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa95xxSA

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of TQMa95xxSA revision 01xx in combination with the MB-SMARC-2 and refers to some software settings. The MB-SMARC-2 serves as an evaluation board for the TQMa95xxSA. A certain TQMa95xxSA derivative does not necessarily provide all features described in this Preliminary User's Manual. This Preliminary User's Manual does also not replace the NXP i.MX 95 Reference Manual (2). The CPU derivatives provide up to six Arm Cortex-A55 cores, Arm Mali GPU, 4K VPU, ISP and ML acceleration NPU.

The TQMa95xxSA is a universal SMARC module based on these NXP ARM® Cortex®-A55 i.MX 95 CPUs, see also Table 3.

An i.MX 95 Cortex®-A55 core typically operates up to 2 GHz.

2.1 Block diagram i.MX 95

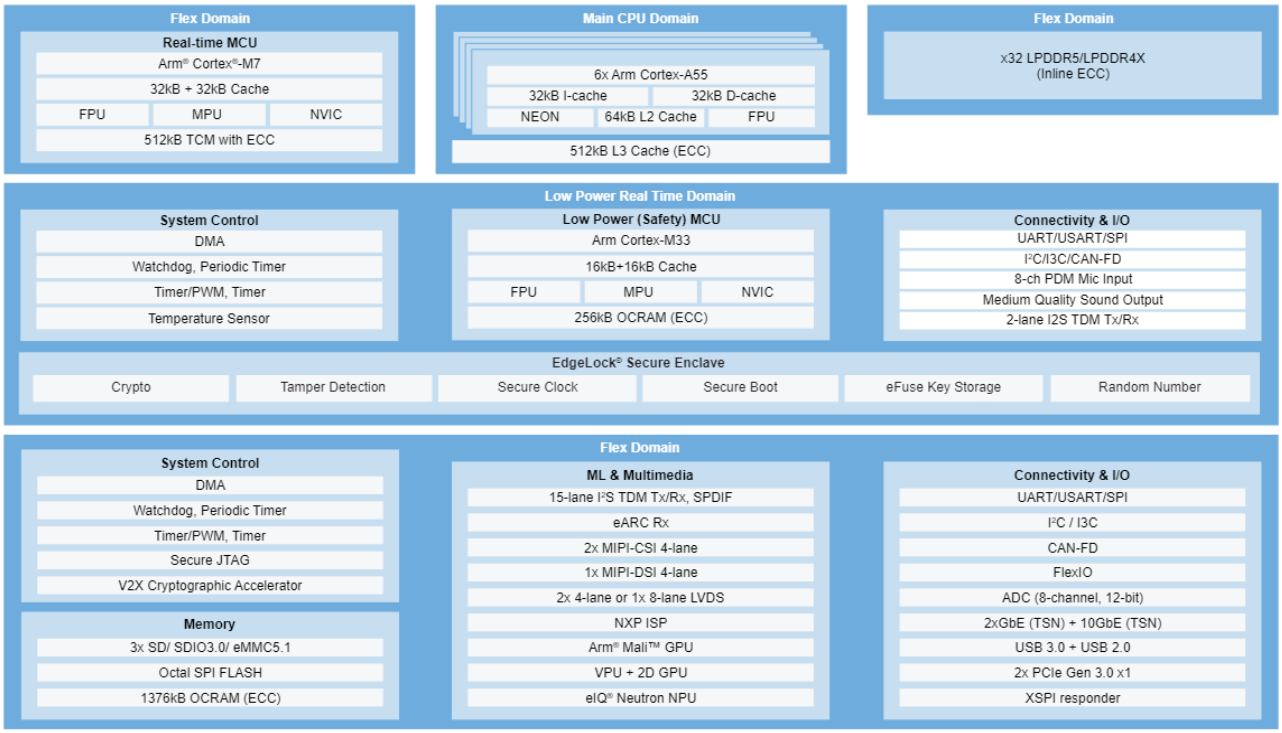


Figure 1: Block diagram i.MX 95 CPU
(Source: NXP)

2.2 Key functions and characteristics

The TQMa95xxSA extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

A suitable i.MX 95 derivative can be selected for each requirement.

The signals are routed to the card edge connector according to SMARC 2.1 standard. All essential components like CPU, LPDDR5 SDRAM, eMMC and power management are already integrated on the TQMa95xxSA. The main features of the TQMa95xxSA are:

- 64-bit NXP i.MX 95 CPU with up to six ARM® Cortex®-A55
- Standard form factor according to SMARC 2.1 (82 mm x 50 mm)
- Interface compatibility according to SMARC 2.1
- x32 RAM in LPDDR5 version
- Quad-SPI NOR flash (optional)
- Customized EEPROM (optional)
- RTC (optional)
- Plug & Trust Secure Element (optional)
- Gyroscope (optional)
- Second Ethernet PHY (optional)
- DisplayPort-Bridge (optional)
- Boot mode selection on TQMa95xxSA
- Voltage range of 3.0 V to 5.25 V (optional: 3.3 V fixed supply voltage)

The IO voltage of most interfaces is set to 1.8 V by the SMARC standard. Signals for differential high-speed interfaces have different standardized IO levels.

3. ELECTRONICS

The information provided in this Preliminary User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa95xxSA and the BSP provided by TQ-Systems GmbH, see also section 5.

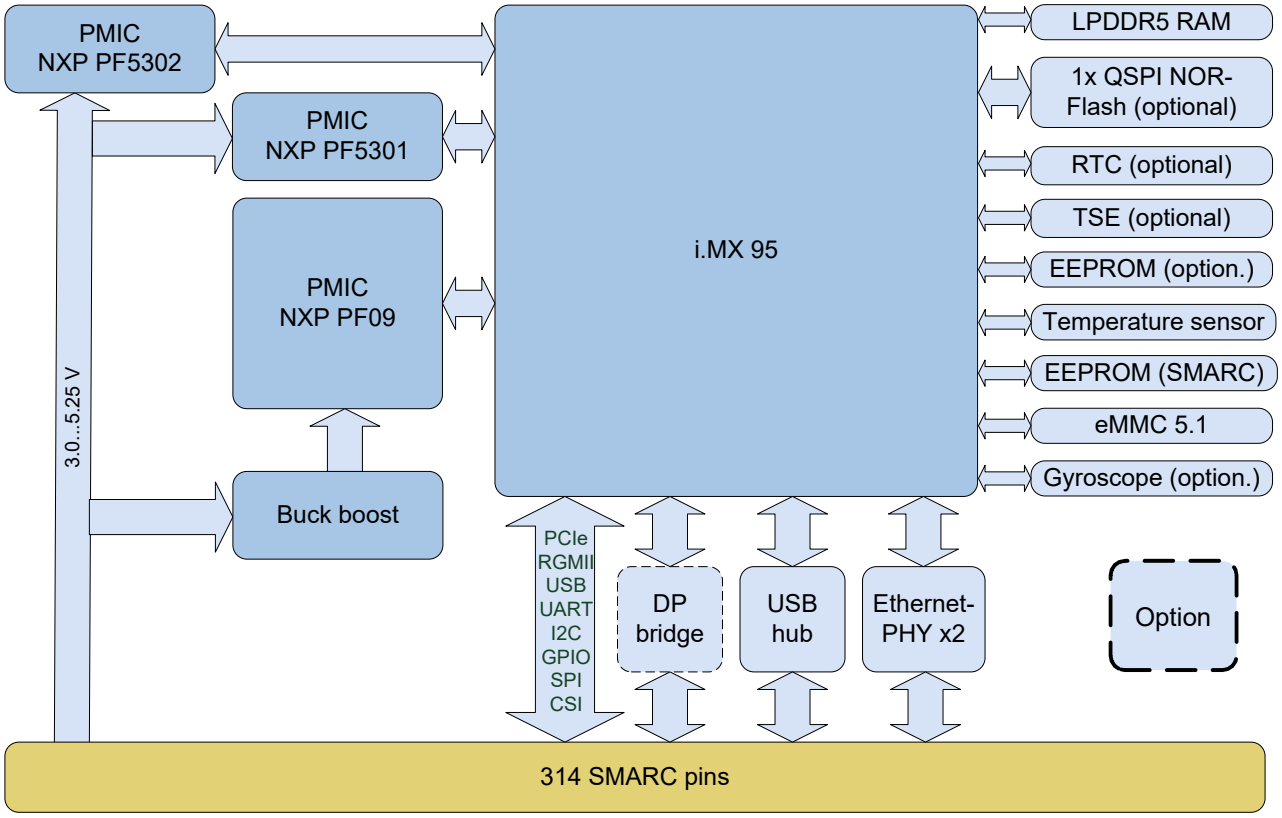


Figure 2: Block diagram TQMa95xxSA

3.1 Interfaces to other systems and devices

The TQMa95xxSA has a SMARC pin strip with a total of 314 pins, divided between the top and bottom side of the board, via which it is connected to the baseboard. Furthermore, the module has four holes with which it can be fixed to the carrier board by means of screws.

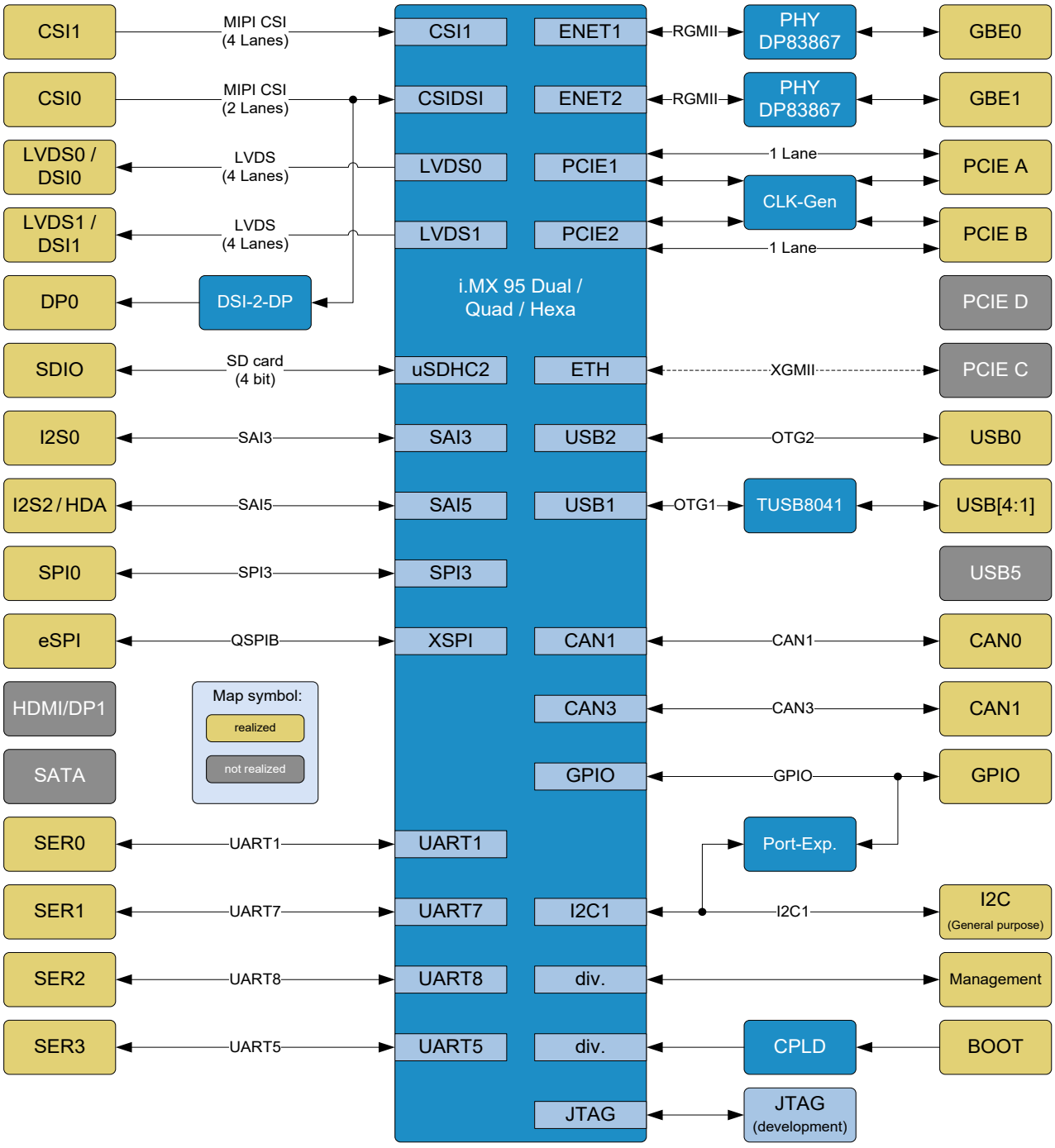


Figure 3: SMARC interface with i.MX 95

3.2 Pin multiplexing

When using the CPU signals, the multiple pin configurations by different CPU-internal function units must be taken note of.

The pin assignment listed in Table 2 refers to the corresponding BSP provided by TQ-Systems GmbH in combination with the MB-SMARC-2.

The electrical and pin characteristics are to be taken from the i.MX 95 Data Sheet (1), the i.MX 95 Reference Manual (2), and the PMIC Data Sheet (4).

Attention: Destruction or malfunction	
	Depending on the configuration, many i.MX 95 balls can provide several different functions. Please take note of the information in the i.MX 95 Reference Manual (2), and the i.MX 95 Errata (3) concerning the configuration of these pins before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa95xxSA. The meanings given in the following tables must be observed: RFU: Reserved pins without function. To support future TQMa95xxSA versions, these pins must not be connected. DNC: These pins must not be connected, they have to be left open. A:Indicates an optional interface, implemented on pins shared with another use

3.3 SMARC connector X1

Table 2: Pinout SMARC connector X1

Ball	Dir.	Level	Group	SMARC signal	Pin		SMARC signal	Group	Level	Dir.	Ball
					–	S1	CSI1_TX+ / I2C_CAM1_CK	CSI1	1.8 V	O	V48
G51	I	1.8 V	CONFIG	SMB_ALERT_1V8#	P1	S2	CSI1_TX- / I2C_CAM1_DAT	CSI1	1.8 V	I/O	V46
-	P	-	Power	GND	P2	S3	GND	Power	-	P	-
E15	O	1.8 V	CSI1	CSI1_CK+	P3	S4	RSVD	-	-	-	-
F16	O	1.8 V	CSI1	CSI1_CK-	P4	S5	CSI0_TX+ / I2C_CAM0_CK	CSI0	1.8 V	O	V44
T48	I/O	3.3 V	GBE1	GBE1_SDP	P5	S6	CAM_MCK	CSI1	1.8 V	O	L49
T46	I/O	3.3 V	GBE0	GBE0_SDP	P6	S7	CSI0_TX- / I2C_CAM0_DAT	CSI0	1.8 V	I/O	U51
E19	I	1.8 V	CSI1	CSI1_RX0+	P7	S8	CSI0_CK+	CSI0	1.8 V	I	B10
F20	I	1.8 V	CSI1	CSI1_RX0-	P8	S9	CSI0_CK-	CSI0	1.8 V	I	C11
-	P	-	Power	GND	P9	S10	GND	Power	-	P	-
E17	I	1.8 V	CSI1	CSI1_RX1+	P10	S11	CSI0_RX0+	CSI0	1.8 V	I	B14
D18	I	1.8 V	CSI1	CSI1_RX1-	P11	S12	CSI0_RX0-	CSI0	1.8 V	I	C15
-	P	-	Power	GND	P12	S13	GND	Power	-	P	-
E13	I	1.8 V	CSI1	CSI1_RX2+	P13	S14	CSI0_RX1+	CSI0	1.8 V	I	B12
D14	I	1.8 V	CSI1	CSI1_RX2-	P14	S15	CSI0_RX1-	CSI0	1.8 V	I	A13
-	P		Power	GND	P15	S16	GND	Power		P	-
E11	I	1.8 V	CSI1	CSI1_RX3+	P16	S17	GBE1_MDI0+	GBE1	-	A	-
F12	I	1.8 V	CSI1	CSI1_RX3-	P17	S18	GBE1_MDI0-	GBE1	-	A	-
-	P	-	Power	GND	P18	S19	GBE1_LINK100#	-	-	-	-
-	A	-	GBE0	GBE0_MDI3-	P19	S20	GBE1_MDI1+	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI3+	P20	S21	GBE1_MDI1-	GBE1	-	A	-
-	-	-	-	GBE0_LINK100#	P21	S22	GBE1_LINK1000#	GBE1	3.3 V	O	-
-	O	3.3 V	GBE0	GBE0_LINK1000#	P22	S23	GBE1_MDI2+	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI2-	P23	S24	GBE1_MDI2-	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI2+	P24	S25	GND	Power	-	P	-
-	O	3.3 V	GBE0	GBE0_LINK_ACT#	P25	S26	GBE1_MDI3+	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI1-	P26	S27	GBE1_MDI3-	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI1+	P27	S28	GBE1_CTREF	-	-	-	-
-	-	-	-	GBE0_CTREF	P28	S29	PCIE_D_TX+/SERDES_0_TX+	-	-	-	-
-	A	-	GBE0	GBE0_MDI0-	P29	S30	PCIE_D_TX-/SERDES_0_TX-	-	-	-	-
-	A	-	GBE0	GBE0_MDI0+	P30	S31	GBE1_LINK_ACT#	GBE1	3.3 V	O	-
L51	O	1.8 V	SPI0	SPI0_CS1#	P31	S32	PCIE_D_RX+/SERDES_0_RX+	-	-	-	-
-	P	-	Power	GND	P32	S33	PCIE_D_RX-/SERDES_0_RX-	-	-	-	-
-	I	1.8 / 3.3 V	SDIO	SDIO_WP	P33	S34	GND	Power	-	P	-
AB52	I/O	1.8 / 3.3 V	SDIO	SDIO_CMD	P34	S35	USB4+	USB4	-	I/O	-
AD48	I	1.8 / 3.3 V	SDIO	SDIO_CD#	P35	S36	USB4-	USB4	-	I/O	-
AB48	O	1.8 / 3.3 V	SDIO	SDIO_CK	P36	S37	USB3_VBUS_DET	USB3	-	-	-
AD52	O	3.3 V	SDIO	SDIO_PWR_EN	P37	S38	AUDIO_MCK	I2S0	1.8 V	O	P48
-	P	-	Power	GND	P38	S39	I2S0_LRCK	I2S0	1.8 V	O	U45
AC51	I/O	1.8 / 3.3 V	SDIO	SDIO_D0	P39	S40	I2S0_SDOUT	I2S0	1.8 V	O	R51
AC49	I/O	1.8 / 3.3 V	SDIO	SDIO_D1	P40	S41	I2S0_SDIN	I2S0	1.8 V	I	R49
AA51	I/O	1.8 / 3.3 V	SDIO	SDIO_D2	P41	S42	I2S0_CK	I2S0	1.8 V	O	P46
AA49	I/O	1.8 / 3.3 V	SDIO	SDIO_D3	P42	S43	ESPI_ALERT0#	eSPI	1.8 V	I	AK44
M44	O	1.8 V	SPI0	SPI0_CS0#	P43	S44	ESPI_ALERT1#	-	-	-	-
M52	O	1.8 V	SPI0	SPI0_CK	P44	S45	MDIO_CLK	SERDES	1.8 V	O	-
M46	I	1.8 V	SPI0	SPI0_DIN	P45	S46	MDIO_DAT	SERDES	1.8 V	I/O	-
M48	O	1.8 V	SPI0	SPI0_DO	P46	S47	GND	Power	-	P	-
-	P	-	Power	GND	P47	S48	I2C_GP_CK	I2C	1.8 V	O	D48
-	-	-	-	SATA_TX+	P48	S49	I2C_GP_DAT	I2C	1.8 V	I/O	D52
-	-	-	-	SATA_TX-	P49	S50	HDA_SYNC / I2S2_LRCK	I2S2	1.8 V	O	AK50
-	P	-	Power	GND	P50	S51	HDA_SDO / I2S2_SDOUT	I2S2	1.8 V	O	AJ49
-	-	-	-	SATA_RX+	P51	S52	HDA_SDI / I2S2_SDIN	I2S2	1.8 V	I	AH50
-	-	-	-	SATA_RX-	P52	S53	HDA_CK / I2S2_CK	I2S2	1.8 V	O	AJ51
-	P	-	Power	GND	P53	S54	SATA_ACT#	-	-	-	-

3.1.2 SMARC connector X1 (continued)

Table 2: Pinout SMARC connector X1 (continued)

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
AJ41	O	1.8 V	eSPI	ESPI_CS0#	P54	S55	USB5_EN_OC#	-	-	-	-
AH42	O	1.8 V	eSPI	ESPI_CS1#	P55	S56	ESPI_IO_2	eSPI	1.8 V	I/O	AJ47
AJ43	O	1.8 V	eSPI	ESPI_CK	P56	S57	ESPI_IO_3	eSPI	1.8 V	I/O	AK48
AH46	I/O	1.8 V	eSPI	ESPI_IO_1	P57	S58	ESPI_RESET#	eSPI	1.8 V	O	-
AJ45	I/O	1.8 V	eSPI	ESPI_IO_0	P58	S59	USB5+	-	-	-	-
-	P	-	Power	GND	P59	S60	USB5-	-	-	-	-
B24	I/O	-	USB0	USB0+	P60	S61	GND	Power	-	P	-
A25	I/O	-	USB0	USB0-	P61	S62	USB3_SSTX+	USB3	-	O	-
-	-	3.3 V	USB0	USB0_EN_OC#	P62	S63	USB3_SSTX-	USB3	-	O	-
E27	I	5 V	USB0	USB0_VBUS_DET	P63	S64	GND	Power	-	P	-
F24	I	1.8 V	USB0	USB0_OTG_ID	P64	S65	USB3_SSRX+	USB3	-	I	-
-	I/O	-	USB1	USB1+	P65	S66	USB3_SSRX-	USB3	-	I	-
-	I/O	-	USB1	USB1-	P66	S67	GND	Power	-	P	-
-	I/O	3.3 V	USB1	USB1_EN_OC#	P67	S68	USB3+	USB3	-	I/O	-
-	P	-	Power	GND	P68	S69	USB3-	USB3	-	I/O	-
-	I/O	-	USB2	USB2+	P69	S70	GND	Power	-	P	-
-	I/O	-	USB2	USB2-	P70	S71	USB2_SSTX+	USB2	-	O	-
-	I/O	3.3 V	USB2	USB2_EN_OC#	P71	S72	USB2_SSTX-	USB2	-	O	-
-	-	-	-	RSVD	P72	S73	GND	Power	-	P	-
-	-	-	-	RSVD	P73	S74	USB2_SSRX+	USB2	-	I	-
-	I/O	3.3 V	USB3	USB3_EN_OC#	P74	S75	USB2_SSRX-	USB2	-	I	-
					Key						
-	O	3.3 V	PCIE1	PCIE_A_RST#	P75	S76	PCIE_B_RST#	PCIE2	3.3 V	O	-
-	I/O	3.3 V	USB4	USB4_EN_OC#	P76	S77	PCIE_C_RST#	-	-	-	-
W51	I/O	3.3 V	PCIE2	PCIE_B_CKREQ#	P77	S78	PCIE_C_RX+/SERDES_1_RX+	SERDES	-	I	AJ13
V52	I/O	3.3 V	PCIE1	PCIE_A_CKREQ#	P78	S79	PCIE_C_RX-/SERDES_1_RX-	SERDES	-	I	AK12
-	P	-	Power	GND	P79	S80	GND	Power	-	P	-
AG15	I/O	-	SERDES	PCIE_C_REFCK+	P80	S81	PCIE_C_TX+/SERDES_1_TX+	SERDES	-	O	AJ17
AF14	I/O	-	SERDES	PCIE_C_REFCK-	P81	S82	PCIE_C_TX-/SERDES_1_TX-	SERDES	-	O	AK16
-	P	-	Power	GND	P82	S83	GND	Power	-	P	-
B30*	O	1.0 V	PCIE1	PCIE_A_REFCK+	P83	S84	PCIE_B_REFCK+	PCIE2	1.0 V	O	B32
C31*	O	1.0 V	PCIE1	PCIE_A_REFCK-	P84	S85	PCIE_B_REFCK-	PCIE2	1.0 V	O	A33
-	P	-	Power	GND	P85	S86	GND	Power	-	P	-
B28	I	1.0 V	PCIE1	PCIE_A_RX+	P86	S87	PCIE_B_RX+	PCIE2	1.0 V	I	B34
A29	I	1.0 V	PCIE1	PCIE_A_RX-	P87	S88	PCIE_B_RX-	PCIE2	1.0 V	I	C35
-	P	-	Power	GND	P88	S89	GND	Power	-	P	-
E29	O	1.0 V	PCIE1	PCIE_A_TX+	P89	S90	PCIE_B_TX+	PCIE2	1.0 V	O	E31
D30	O	1.0 V	PCIE1	PCIE_A_TX-	P90	S91	PCIE_B_TX-	PCIE2	1.0 V	O	F32
-	P	-	Power	GND	P91	S92	GND	Power	-	P	-
-	-	-	-	HDMI_D2+ / DP1_LANE0+	P92	S93	DP0_LANE0+	DP	-	O	-
-	-	-	-	HDMI_D2- / DP1_LANE0-	P93	S94	DP0_LANE0-	DP	-	O	-
-	P	-	Power	GND	P94	S95	DP0_AUX_SEL	DP	-	I	-
-	-	-	-	HDMI_D1+ / DP1_LANE1+	P95	S96	DP0_LANE1+	DP	-	O	-
-	-	-	-	HDMI_D1- / DP1_LANE1-	P96	S97	DP0_LANE1-	DP	-	O	-
-	P	-	Power	GND	P97	S98	DP0_HPD	DP	-	I	-
-	-	-	-	HDMI_D0+ / DP1_LANE2+	P98	S99	DP0_LANE2+	-	-	-	-
-	-	-	-	HDMI_D0- / DP1_LANE2-	P99	S100	DP0_LANE2-	-	-	-	-
-	P	-	Power	GND	P100	S101	GND	Power	-	P	-
-	A	-	-	HDMI_CK+ / DP1_LANE3+	P101	S102	DP0_LANE3+	-	-	-	-
-	A	-	-	HDMI_CK- / DP1_LANE3-	P102	S103	DP0_LANE3-	-	-	-	-
-	P	-	Power	GND	P103	S104	USB3_OTG_ID	USB3	-	-	-
-	-	-	-	HDMI_HPD / DP1_HPD	P104	S105	DP0_AUX+	DP	3.3 V	I/O	-
-	-	-	-	HDMI_CTRL_CK / DP1_AUX+	P105	S106	DP0_AUX-	DP	3.3 V	I/O	-

3.1.2 SMARC connector X1 (continued)

Table 2: Pinout SMARC connector X1 (continued)

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
-	-	-	-	HDMI_CTRL_DAT / DP1_AUX-	P106	S107	LCD1_BKLT_EN	LVDS1	1.8 V	O	-
-	-	-	-	DP1_AUX_SEL	P107	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1	1.8 V	O	D2
-	I/O	1.8 V	GPIO	GPIO0 / CAM0_PWR#	P108	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1	1.8 V	O	D4
-	I/O	1.8 V	GPIO	GPIO1 / CAM1_PWR#	P109	S110	GND	Power	-	P	-
-	I/O	1.8 V	GPIO	GPIO2 / CAM0_RST#	P110	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1	1.8 V	I/O	B2
-	I/O	1.8 V	GPIO	GPIO3 / CAM1_RST#	P111	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1	1.8 V	I/O	A3
-	I/O	1.8 V	GPIO	GPIO4 / HDA_RST#	P112	S113	eDP1_HPD	-	-	-	-
R45	I/O	1.8 V	GPIO	GPIO5 / PWM_OUT	P113	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1	1.8 V	I/O	C1
T44	I/O	1.8 V	GPIO	GPIO6 / TACHIN	P114	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1	1.8 V	I/O	C3
H46	I/O	1.8 V	GPIO	GPIO7	P115	S116	LCD1_VDD_EN	LVDS1	1.8 V	O	-
G49	I/O	1.8 V	GPIO	GPIO8	P116	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1	1.8 V	I/O	E1
H48	I/O	1.8 V	GPIO	GPIO9	P117	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1	1.8 V	I/O	E3
-	I/O	1.8 V	GPIO	GPIO10	P118	S119	GND	Power	-	P	-
-	I/O	1.8 V	GPIO	GPIO11	P119	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1	1.8 V	I/O	F2
-	P	-	Power	GND	P120	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1	1.8 V	I/O	F4
E43	O	1.8 V	I2C	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	LVDS1	1.8 V	O	L45
E45	I/O	1.8 V	I2C	I2C_PM_DAT	P122	S123	GPIO13	GPIO	1.8 V	I/O	-
-	I	1.8 V	BOOT	BOOT_SEL0#	P123	S124	GND	Power	-	P	-
-	I	1.8 V	BOOT	BOOT_SEL1#	P124	S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0	1.8 V	I/O	G7
-	I	1.8 V	BOOT	BOOT_SEL2#	P125	S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0	1.8 V	I/O	G9
D42	O	1.8 V	CONFIG	RESET_OUT#	P126	S127	LCD0_BKLT_EN	LVDS0	1.8 V	O	-
D42	I	1.8 V	CONFIG	RESET_IN#	P127	S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0	1.8 V	I/O	F6
F40	I	1.8 V	CONFIG	POWER_BTN#	P128	S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0	1.8 V	I/O	F8
F52	O	1.8 V	SER	SER0_TX	P129	S130	GND	Power	-	P	-
E49	I	1.8 V	SER	SER0_RX	P130	S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0	1.8 V	I/O	D6
F48	O	1.8 V	SER	SER0_RTS#	P131	S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0	1.8 V	I/O	E7
E51	I	1.8 V	SER	SER0_CTS#	P132	S133	LCD0_VDD_EN	LVDS0	1.8 V	O	-
-	P	-	Power	GND	P133	S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0	1.8 V	O	B4
Y48	O	1.8 V	SER	SER1_TX	P134	S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0	1.8 V	O	A5
Y52	I	1.8 V	SER	SER1_RX	P135	S136	GND	Power	-	P	-
N45	O	1.8 V	SER	SER2_TX	P136	S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0	1.8 V	I/O	D8
N49	I	1.8 V	SER	SER2_RX	P137	S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0	1.8 V	I/O	E9
P44	O	1.8 V	SER	SER2_RTS#	P138	S139	I2C_LCD_CK	I2C	1.8 V	O	K52
N51	I	1.8 V	SER	SER2_CTS#	P139	S140	I2C_LCD_DAT	I2C	1.8 V	I/O	K48
J49	O	1.8 V	SER	SER3_TX	P140	S141	LCD0_BKLT_PWM	LVDS0	1.8 V	O	K46
J51	I	1.8 V	SER	SER3_RX	P141	S142	GPIO12	GPIO	1.8 V	I/O	-
-	P	-	Power	GND	P142	S143	GND	Power	-	P	-
F46	O	1.8 V	CAN	CAN0_TX	P143	S144	eDP0_HPD	-	-	-	-
G45	I	1.8 V	CAN	CAN0_RX	P144	S145	WDT_TIME_OUT#	WDOG	1.8 V	O	J45
AK20	O	1.8 V	CAN	CAN1_TX	P145	S146	PCIE_WAKE#	PCIE	3.3 V	I	-
AJ21	I	1.8 V	CAN	CAN1_RX	P146	S147	VDD_RTC	Power	3.0 V	P	-
-	P	3.0…5.25 V	Power	VDD_IN	P147	S148	LID#	CONFIG	1.8 V	I	-
-	P	3.0…5.25 V	Power	VDD_IN	P148	S149	SLEEP#	CONFIG	1.8 V	I	P52
-	P	3.0…5.25 V	Power	VDD_IN	P149	S150	VIN_PWR_BAD#	CONFIG	VDD_IN	I	-
-	P	3.0…5.25 V	Power	VDD_IN	P150	S151	CHARGING#	CONFIG	1.8 V	I	-
-	P	3.0…5.25 V	Power	VDD_IN	P151	S152	CHARGER_PRSNT#	CONFIG	1.8 V	I	-
-	P	3.0…5.25 V	Power	VDD_IN	P152	S153	CARRIER_STBY#	CONFIG	1.8 V	O	C43
-	P	3.0…5.25 V	Power	VDD_IN	P153	S154	CARRIER_PWR_ON	CONFIG	1.8 V	O	-
-	P	3.0…5.25 V	Power	VDD_IN	P154	S155	FORCE_RECOV#	BOOT	1.8 V	I	-
-	P	3.0…5.25 V	Power	VDD_IN	P155	S156	BATLOW#	CONFIG	1.8 V	I	-
-	P	3.0…5.25 V	Power	VDD_IN	P156	S157	TEST#	CONFIG	1.8 V	-	-
						S158	GND	Power	-	P	-

The pins assignment listed in Table 2 refers to the corresponding BSP provided by TQ-Systems GmbH.
For information regarding I/O pins in Table 2 refers to the i.MX 95 Data Sheet (1).

3.4 i.MX 95 CPU

3.4.1 i.MX 95 derivatives

Depending on the TQMa95xxSA version, one of the following i.MX 95 derivatives is assembled.

Table 3: i.MX 95 derivatives

TQMa95xxSA variant	CPU derivative	Cortex®-A55 clock	Cortex®-M33 clock	Cortex®-M7 clock	T_J, temperature range
TQMa9554SA-AA	i.MX9554	4 x 1.8 GHz	250 MHz	800 MHz	-40°C to 105°C
TQMa9556SA-AA	i.MX9556	6 x 1.8 GHz	250 MHz	800 MHz	-40°C to 105°C
TQMa9594SA-AA	i.MX9594	4 x 1.8 GHz	250 MHz	800 MHz	-40°C to 105°C
TQMa9596SA-AA	i.MX9596	6 x 1.8 GHz	250 MHz	800 MHz	-40°C to 105°C

3.4.2 i.MX 95 errata

Attention: Malfunction	
	Please take note of the current i.MX 95 errata (3).

3.4.3 Boot modes

After the release of IMX_POR# the system controller (SCU) boots from the internal ROM. Depending on the OPT fuses (eFuse) and the boot mode settings of the system controller the system boots from the selected boot source. The following interfaces are available as boot source:

- eMMC
- Serial downloader
- SD card

The SMARC standard requires, depending on the selected boot mode, a defined wiring of the SMARC connector pins BOOT_SEL[2:0]. These are converted with a CPLD to the boot mode pins BOOT_MODE[3:0]. As the boot mode pins of the i.MX 95 are multiplexed to signals of other functions, an additional analog switch is provided between the CPLD and CPU, which switches off the CPLD signals after a defined time.

The FORCE_RECOV# signal is used to switch to the "Force Recovery" mode or "Serial Downloader", see (1) and (6).

More information about boot interfaces and its configuration is to be taken from the i.MX 95 Data Sheet (1) and the i.MX 95 Reference Manual (2). Alternatively, an image can be loaded into the internal RAM via serial downloader.

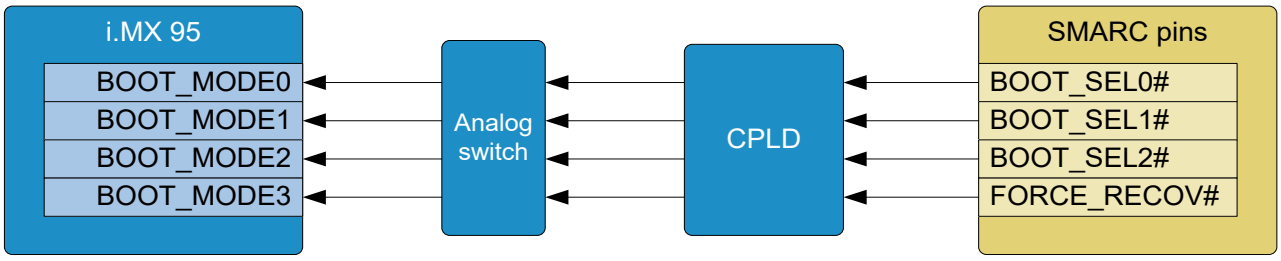


Figure 4: Block diagram Boot-Mode

The following boot media are provided according to the SMARC standard:

Table 4: Boot sources

i.MX 95 BOOT_MODE[3:0]	FORCE_RECOV#	BOOT_SEL[2:0]# [1]	Boot Source
1000	1	101	Remote / Internal eFuses. (set as “Boot from Fuses”, as i.MX 95 does not define a remote mode)
1001	0	xxx	Recovery mode / serial downloader
1010	1	110	eMMC
1011	1	001	SD card
1110	1	100	FlexSPI NAND 4k (QSPI NOR flash)

Note: Field software updates	
	When designing a carrier board, it is recommended to have a redundant update concept for field software updates.

3.5 Memory

3.6 RAM

LPDDR5-RAM with a memory width of 32 bits is used on the TQMa95xxSA. The i.MX 95 supports Inline ECC.
The LPDDR memory interface has the following basic parameters:

Table 5: Parameter RAM interface

Parameter	i.MX 95
Memory type	LPDDR4X / LPDDR5
DDR timing	max. LPDDR5-6400
DDR clock frequenz	max. 3200 MHz
Bus width (data)	32 bit
Max. memory size	16 GByte

The standard memory size of the TQMa95xxSA is 2 GByte. Variants with 4 GByte and 8 GByte are available.

Attention: Malfunction	
	The TQMa95xxSA uses a specially developed RAM timing. Each memory expansion level required its own RAM configuration.

1: Floating inputs are taken as "1" due to the pull-up on the TQMa95xxSA.

3.7 eMMC

An eMMC is available on the TQMa95xxSA as non-volatile memory for programs and data (e.g. bootloader, operating system, application). The following figure shows the interface of the eMMC to the i.MX 95:

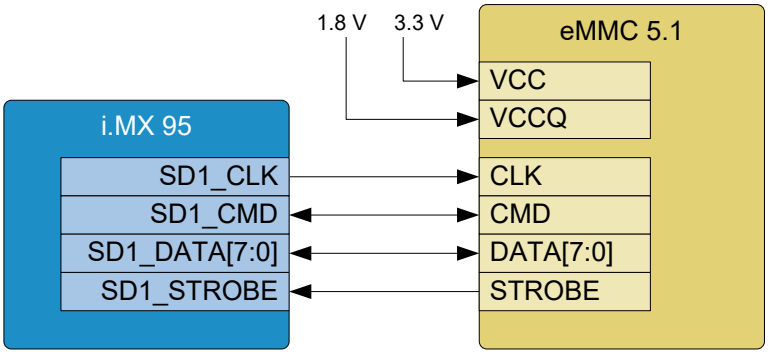


Figure 5: Block diagram eMMC

The eMMC is connected via the USDHC1 interface of the i.MX 95. A maximum transfer rate of 400 MB/s is supported, which corresponds to HS400 mode. Series resistors are provided for the CLK, DATA and CMD signals.

The standard eMMC is SanDisks SDINBDG4-8G-XI2 (8 GByte / MLC).

3.8 NOR flash

The i.MX 95 offers another interface, USDHC3, which can be used for memory connection. A Quad-SPI flash is connected to this interface, the implementation of which is based on other modules. 33 Ω series resistors are provided in the data lines. The supply voltage of this flash is 1.8 V.

The standard NOR flash is Winbond W25Q512NWBIQ (64 MByte).

3.9 EEPROM

The TQMa95xxSA has two EEPROMs, one customer specific and one SMARC specific. Both are connected to the I2C_GP bus of the TQMa95xxSA and are supplied with 1.8 V.

The I^2C address of the SMARC-specific EEPROM is set to `0x50` according to the specification. Information about the module configuration can be found at this address.

The second EEPROM is optional and can be used for customer specific data.

The following table shows details of the default EEPROM:

Table 6: EEPROM

Manufacturer	Part number	Size	Temperature range
ST Microelectronics	M24C64-DFMC6TG	64 Kbit	–40 °C to +85 °C

3.10 Temperature sensor

A temperature sensor (Texas Instruments TMP1075DSGR), controlled by the I2C1 bus (address: 0x4A), is assembled. The ALERT alarm output is routed to a GPIO expander.

3.11 i.MX 95 internal RTC

The i.MX 95 has an internal RTC. Its accuracy is primarily determined by the characteristics of the quartz used. The type FC-135 used on the TQMa95xxSA has a standard frequency tolerance of ±20 ppm at +25 °C. (Parabolic coefficient: max. -0.04 x 10^{-6} / $°C^2$)

3.12 Optional RTC PCF85063

In addition to the i.MX 95 internal RTC, TQMa95xxSA variants with discrete RTC at I2C_GP are available. It is recommended to use the RTC PCF85063 due to the lower current consumption during standby modes.
Unlike the temperature sensor, its interrupt signal is routed directly to a CPU pin. This means that the CPU can be woken up directly by the RTC from any standby mode.

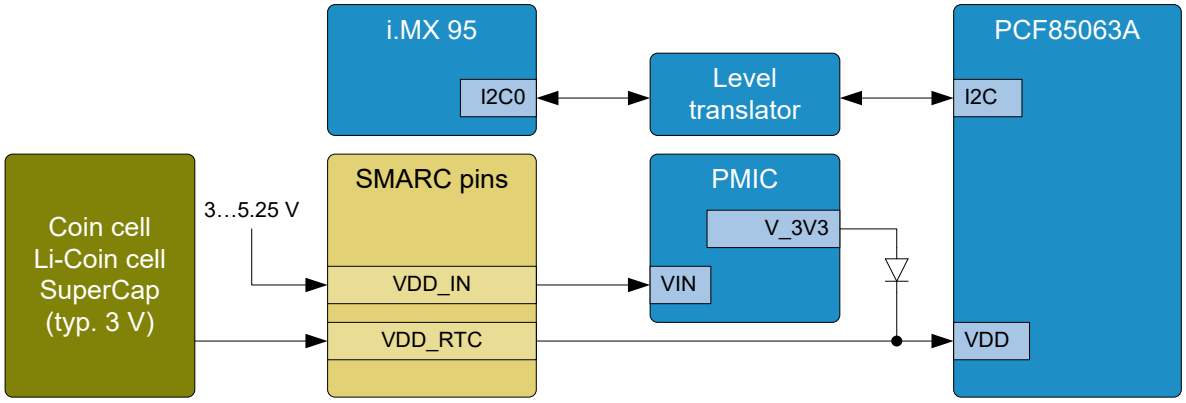


Figure 6: Block diagram RTC supply (TQMa95xxSA with discrete RTC)

The RTC PCF85063 is only supplied directly by VDD_RTC when the PMIC is switched off or the module supply is switched off. During runtime the PMIC takes over the supply via the modules supply voltage of 3.3 V.

- The discrete RTC has I2C_GP address `0x51 / 101 0001b`

3.13 Gyroscope

An optional gyroscope with I2C and SPI interfaces is provided on the TQMa95xxSA. It allows to determine the position of the TQMa95xxSA. It is connected via I2C_GP (address: `0x6B`).

3.14 1G Ethernet

Two Gigabit Ethernet interfaces (GBE0, GBE1) are provided at the SMARC connector of the TQMa95xxSA.
These are implemented with two independent PHYs. According to the SMARC standard, the Ethernet PHYs are part of the SMARC module, so that only the magnatics are implemented on the carrier.

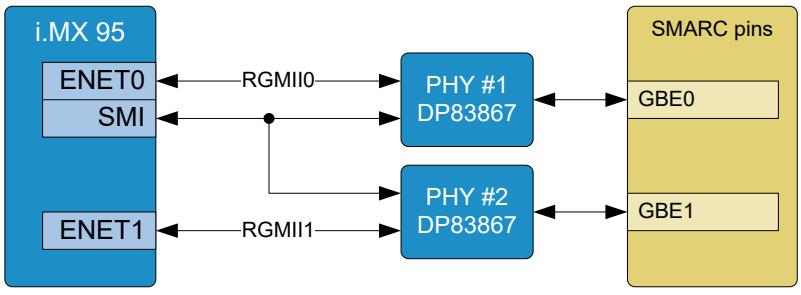


Figure 7: Block diagram 1G Ethernet

3.15 10G Ethernet

The SMARC standard allows the PCIE_C or PCIE_D interfaces to be alternatively assigned to SERDES interfaces. However, the standard itself states that SGMII or XGMII interfaces are most commonly used on these pins. Unfortunately, no more precise requirements are defined for these use cases. For this reason, an alternative assignment of these pins with the signals of the 10G Ethernet interface of the CPU is provided. As the correct assignment cannot be completely guaranteed, all signals are provided with unassembled 0R resistors and are therefore isolated.

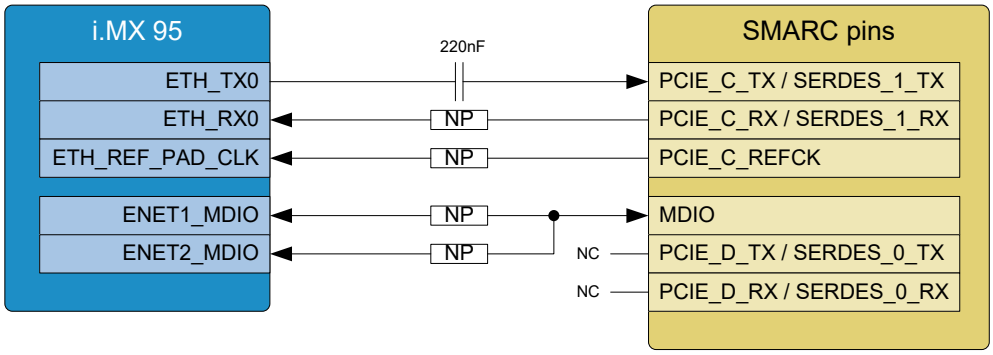


Figure 8: Block diagram 10G Ethernet

3.16 USB

A USB 3.0 hub is used to operate most of the USB interfaces provided in the SMARC standard. It is connected to the USB1 interface of the i.MX 95, as only this interface has the necessary SuperSpeed signals. However, as the USB1 interface is also intended for serial download mode, the USB 2.0 data lines of this interface can be switched via an analog switch.

The USB3 port can only be used as a host because the USB hub does not support dual role.

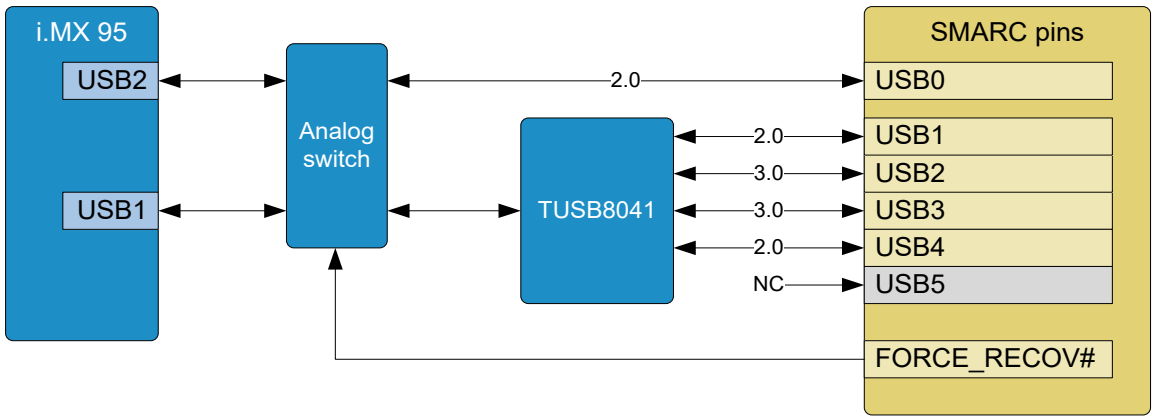


Figure 9: Block diagram USB interfaces

3.17 LVDS

The i.MX 95 offers two four-channel LVDS interfaces. These are connected directly to the corresponding SMARC pins without any further wiring. The LVDS control signals BKLT_EN and VDD_EN are provided by outputs from the port expanders, while the PWM signals BKLT_PWM are provided by PWM-capable signals from the CPU.

I2C6 is used as the I2C bus for communication with the displays.

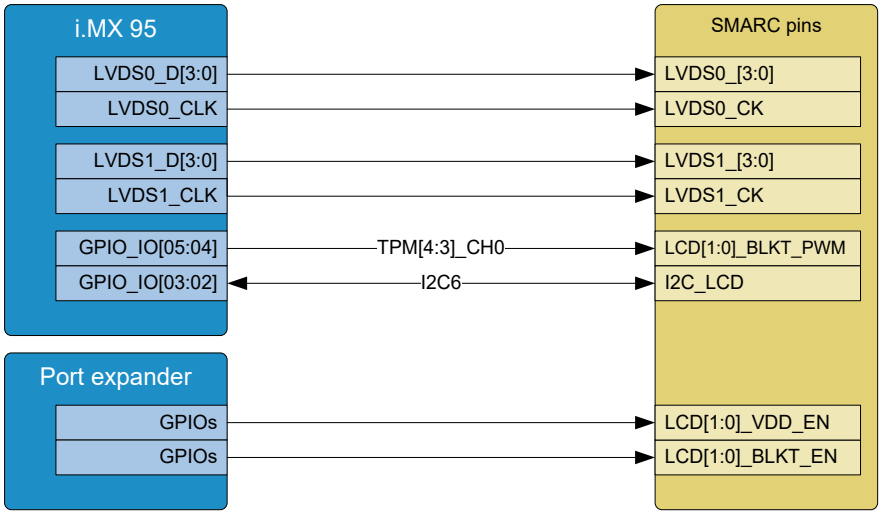
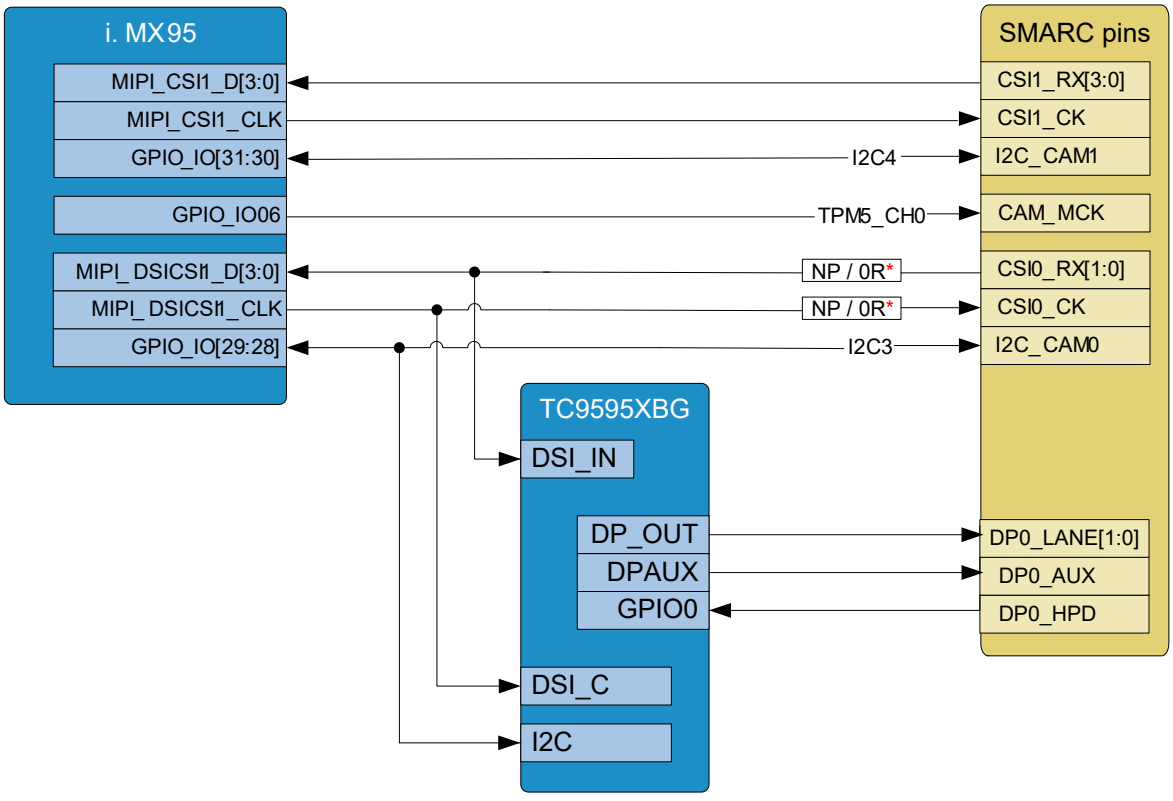


Figure 10: Block diagram LVDS

3.18 DSI / DisplayPort

The combined CSIDSI interface of the i.MX 95 is converted via an optional DisplayPort bridge (TC9595XBG TOSHIBA / VESA® DisplayPortTM 1.1a Standard / WUXGA (1900 x 1200 @ 24bit)) and made available on the corresponding SMARC pins. Note that the bridge only provides a two-channel DisplayPort. The other channels remain unconnected.



* The resistors are not installed when the optional DP bridge is installed.

Figure 11: Block diagram DisplayPort und CSI

The CPU signals are additionally connected to the SMARC CSI0 pins with 0R bridges to serve as a second CSI interface if the DisplayPort bridge is not installed. In this case, the DisplayPort signals are not available (see following chapter).

3.19 Camera Serial Interface (CSI)

The CPU provides up to two CSI interfaces, one of which can also be used as a DSI interface and is therefore primarily intended for connecting the DisplayPort bridge (see previous chapter). The CSI0 pins are connected to the CPU with 0R resistors. They can be used as a camera interface if no DisplayPort bridge is installed.

The CPU's dedicated CSI interface is connected to the CSI1 pins of the SMARC connector.

CSI1 uses all four data lanes of the CPU, while CSI0 uses only two. Both camera interfaces have independent I2C buses that are always connected directly to the SMARC pins. I2C_CAM0 is also connected to the DisplayPort bridge.

3.20 SD card interface

The SD Card interface is provided by the USDHC2 interface of the i.MX 95. The SMARC-signal SDIO_PWR_EN is used to switch on the SD supply voltage on the carrier. In order to boot from the SD card, a high level must be applied to this signal at boot time. The TQMa95xxSA provides the necessary circuitry.

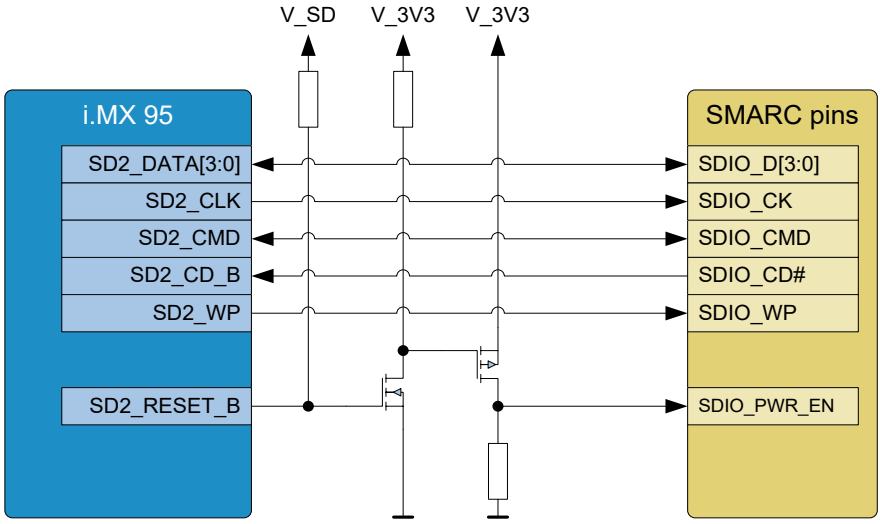


Figure 12: Block diagram SDIO

3.21 Audio (I2S)

The I2S0 interface on the SMARC pins is provided by the SAI3 interface of the i.MX 95. The SAI3 interface is also connected to the DisplayPort bridge as an assembly option, but is not connected to it by default. In addition, the I2S2 interface is connected to the CPU via SAI5.

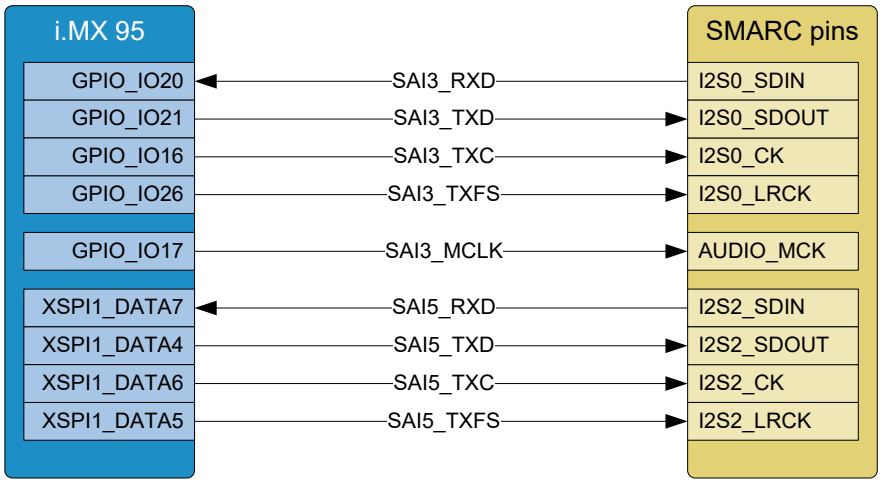


Figure 13: Block diagram Audio

3.22 SPI

For the SPI0 interface of the SMARC pins, GPIO balls of the i.MX 95 are used. Two chip select signals are provided.

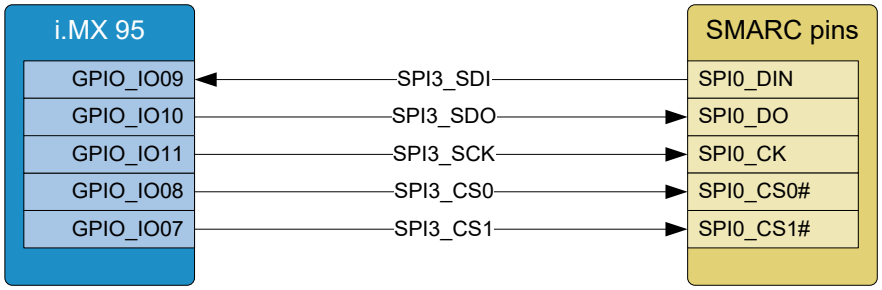


Figure 14: Block diagram SPI

3.23 eSPI

The eSPI pins are connected to the FlexSPI interface of the i.MX 95. As this is not an eSPI interface according to the Intel standard, there may be functional restrictions. ESPI_RESET# is provided as an output signal by one of the port expanders. The signal E-SPI_ALERT0# is realized by the CPU via interrupt capable GPIO. ESPI_ALERT1# is not used.

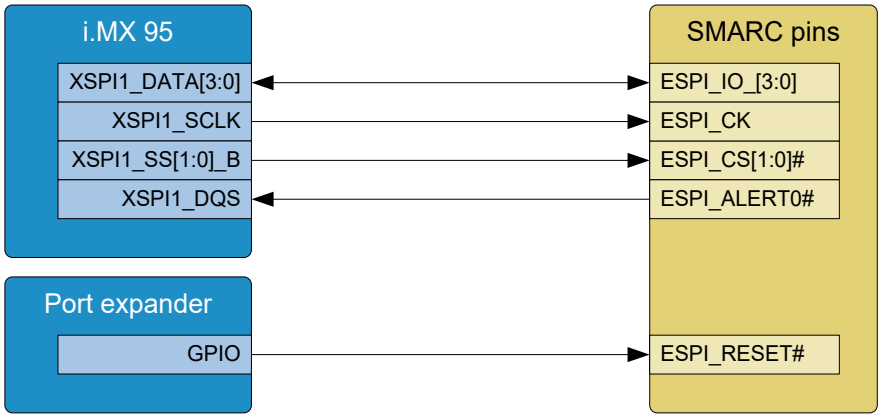


Figure 15: Block diagram eSPI

3.24 Serial ports

Due to the large number of possible UART interfaces of the i.MX 95 and its various sub-CPUs, all four possible serial interfaces of the SMARC pins are connected, including SER3...1 directly. SER0 is partially routed via an analog switch, as some of the signals used act as boot mode signals. The corresponding signal switching happens automatically when the module is started and should therefore not affect normal operation.

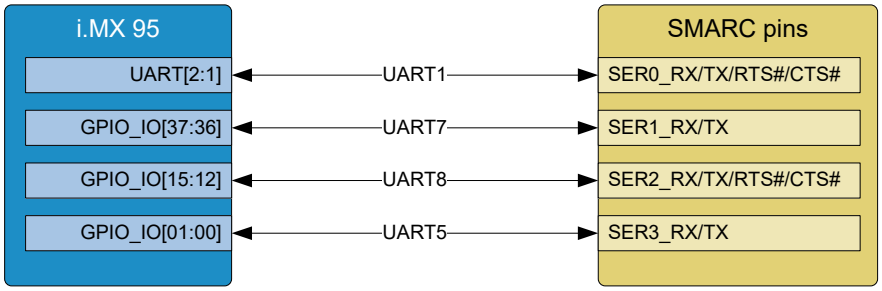


Figure 16: Block diagram Serial Ports

3.25 CAN bus

Both CAN interfaces are provided at the SMARC pins. The i.MX 95 uses CAN1 and CAN3 for this purpose.

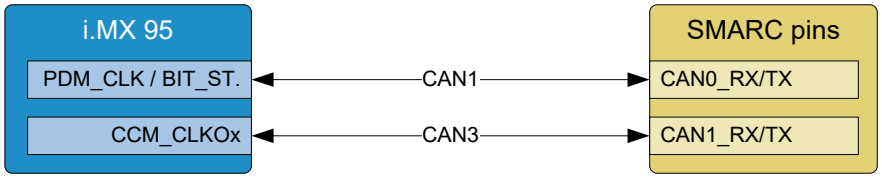


Figure 17: Block diagram CAN

3.26 PCI Express

A total of four PCIe interfaces are provided in the SMARC standard, of which only PCIE_A and PCIE_B are provided by the i.MX 95. PCIE_C and PCIE_D of the SMARC pins are not assigned to PCIe. Due to the internal CPU circuitry, the clock must be supplied from an external source. For this reason, a PCIe clock generator is provided on the TQMa95xxSA. This is connected via I2C and can control each channel separately. Two control signals are used for this via port expanders.

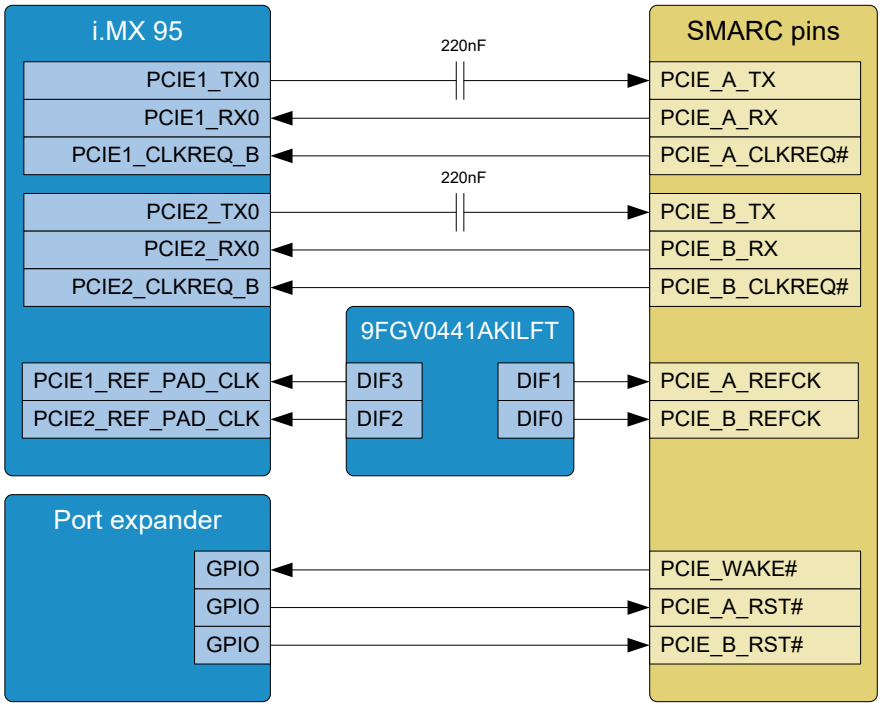


Figure 18: Block diagram PCI Express

As there is a discrepancy between the IO level of the CPU and the SMARC standard, a level translator is provided for the CLKREQ# and RST# signals at each channel. Due to the limited number of CPU IOs, the RST# signals are provided via port expanders. The clock generator is also controlled via I2C and port expander IOs.

3.27 I²C

The I²C interfaces of the i.MX 95 are provided at the SMARC connector as follows:

Table 7: I²C interface

SMARC pins	i.MX 95 interface
I2C_GP	I2C1
I2C_PM	I2C2
I2C_CAM0	I2C3
I2C_CAM1	I2C4
I2C_LCD	I2C6

Standard-compliant pull-up resistors are provided on all I²C signals on the TQMa95xxSA.

The following table shows the addresses of the I²C devices used on the TQMa95xxSA:

Table 8: I²C addresses

Bus	I2C-Device	Address	Remark
I2C1 (I2C_GP)	EEPROM	0x50	SMARC specific
	EEPROM ID-Page	0x58	SMARC specific
	EEPROM	0x54	Customer specific
	EEPROM ID-Page	0x5C	Customer specific
	RTC PCF85063	0x51	
	TSE SE050	0x48	Not placed by default
	Temperature sensor TMP1075	0x4A	
	Port expander 1	0x75	
	Port expander 2	0x74	
	PCIE clock generator	0x6A	
	USB hub	0x44	Not connected by default
	Gyroskop	0x6B	Not placed by default
I2C_CAM0 / DSI0_I2C	Display-Port-Bridge	0x0F	
I2C2 (I2C_PM)	PMIC PF090x	0x08	
	PMIC PF5301	0x2A	
	PMIC PF5302	0x29	

3.28 GPIO

The SMARC standard specifies a total of 14 GPIOs. The standard recommends to use GPIO0...5 preferably as output and GPIO6...13 preferably as input. The i.MX 95 GPIOs can be used in both directions.

The native GPIOs of the i.MX 95 enable use in both directions. However, due to the CPU interface assignment and limited number of pins, not all 14 GPIOs can be connected directly to the CPU. The majority of these pins are therefore provided via port expanders. A corresponding overview can be found in the following table.

A special alternative use is provided for GPIO5 and GPIO6, which can be multiplexed as a PWM output or tachometer input.

Table 9: GPIO pins and alternative functions

SMARC pin	Origin (IC)	IC GPIO	Preferred direction	Alternative use
GPIO0 / CAM0_PWR#	Port expander 1	P14	Output	-
GPIO1 / CAM1_PWR#	Port expander 1	P15	Output	-
GPIO2 / CAM0_RST#	Port expander 1	P16	Output	-
GPIO3 / CAM1_RST#	Port expander 1	P17	Output	-
GPIO4 / HDA_RST#	Port expander 2	P01	Output	-
GPIO5 / PWM_OUT	i.MX 95	GPIO_IO19	Output	TPM6_CH2
GPIO6 / TACHIN	i.MX 95	GPIO_IO22	Input	TPM6_EXTCLK
GPIO7	i.MX 95	GPIO1_IO10	Input	M33_NMI
GPIO8	i.MX 95	GPIO1_IO11	Input	BOOT_MODE2
GPIO9	i.MX 95	GPIO1_IO13	Input	BOOT_MODE3
GPIO10	Port expander 1	P00	Input	-
GPIO11	Port expander 1	P01	Input	-
GPIO12	Port expander 1	P02	Input	-
GPIO13	Port expander 1	P03	Input	-

All GPIOs are provided with discrete pull-up resistors in accordance with the SMARC specification.

3.29 Watchdog

The watchdog signal WDOG_ANY of the i.MX 95 is connected to the watchdog input of the PMIC and to the SMARC pin WDT_TIME_OUT#. Both can be disconnected via 0R resistor.

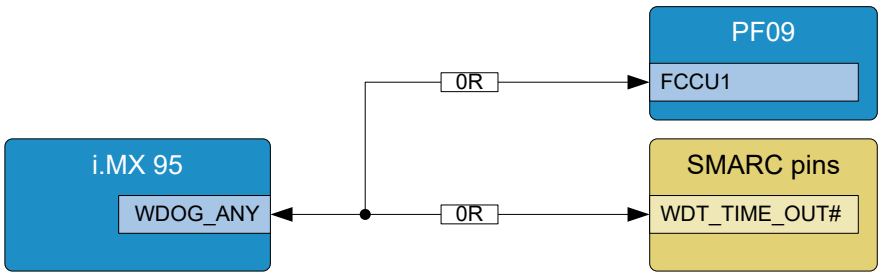


Figure 19: Block diagram Watchdog

3.30 JTAG

The JTAG interface of the i.MX 95 is provided with an optional connector (JST SM10B-SRSS-TB) on the TQMa95xxSA.
The optional connector and the pin assignment are defined in the SMARC specification (6). However, this connector is not assembled by default.

Table 10: Pin assignment JTAG connector

Pin	Name (SMARC spec.)	I/O	TQMa95xxSA-Signal
1	VDD_JTAG_IO	P	V_1V8
2	JTAG_TRST#	-	NC
3	JTAG_TMS	I	JTAG_TMS
4	JTAG_TDO	O	JTAG_TDO
5	JTAG_TDI	I	JTAG_TDI
6	JTAG_TCK	I	JTAG_TCK
7	JTAG_RTCK	I	NC
8	GND	P	GND
9	MFG_MODE#	I	NC
10	GND	P	GND

3.31 Trust Secure Element

Depending on the module variant, a Trust Secure Element (TSE) is available on the TQMa95xxSA. This is connected to the I2C_GP bus (address: `0x48`). The selected chip SE050 from NXP provides additional smartcard interfaces according to ISO14443 and ISO7816 besides the I2C interface. The connection of the antenna for ISO 14443 or the sensor for ISO 7816 must be made on the baseboard.
As the SMARC standard does not provide any pins for these smartcard interfaces, the signals for the interfaces in accordance with ISO14443 and ISO7816 are routed to the unused SMARC pins of the HDMI interface but are disconnected by default using unplaced 0R resistors.

Table 11: SE050 pin assignment on SMARC connector

Signal SE050	SMARC-Pin
ISO_14443_LA	P101 – HDMI_CK+
ISO_14443_LB	P102 – HDMI_CK-
ISO_7816_IO1	P92 – HDMI_D2+
ISO_7816_IO2	P93 – HDMI_D2-
ISO_7816_CLK	P96 – HDMI_D1-
ISO_7816_RST	P95 – HDMI_D1+

If the SE050 is equipped as an option, but no ISO14443 and ISO7816 devices are to be operated, the signals on the motherboard are to be wired as follows:

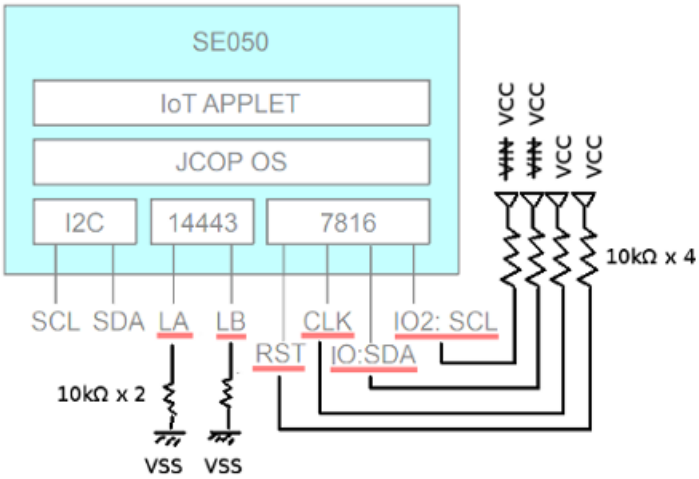


Figure 20: Connecting the NC-Pins

(Source: NXP)

3.32 Unused CPU signals

CPU signals that cannot be mapped using the SMARC standard are either terminated directly on the module or left unconnected. These are mainly signals of the function groups ADC_IN, EARC and Tamper.

According to the pinout of the CPU, the corresponding CPU balls have no alternative function and therefore cannot be used as GPIOs or similar.

3.33 Power

The SMARC specification specifies a power supply range of 3.0 V to 5.25 V, although this can be further restricted (e.g. to a fixed 3.3 V (3.1 V to 3.4 V)). All supply voltages required by the CPU and the module components are generated by the TQMa95xxSA.

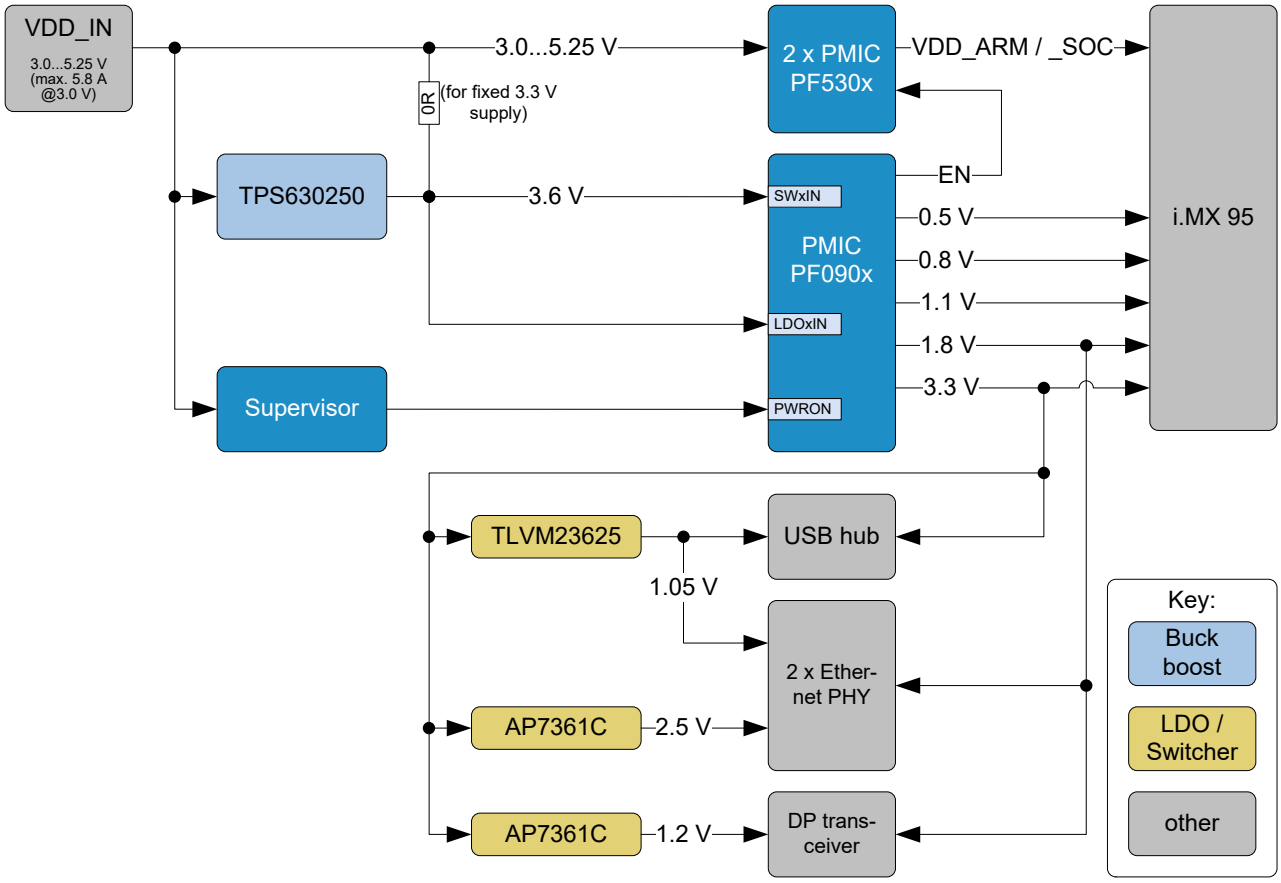


Figure 21: Block diagram module supply

Powering mainboard components from the SMARC module is not applicable as this is not defined in the SMARC specification. As the supply of the module is defined in the SMARC standard with a permissible voltage range and fixed pin assignment, no measures are provided with regard to reverse polarity protection or inrush currents.
ESD and overvoltage protection, e.g. TVS diodes, are not implemented on the module. Appropriate solutions must always be provided on the carrier boards.

3.33.1 V_VDD_RTC

The SMARC pin V_VDD_RTC allows the connection to a coin cell to supply the optional RTC (see chapter 3.13). The voltage range is 2.0 V to 3.25 V according to SMARC specification.

Table 12: Current consumption of discrete RTC

Voltage V_VDD_RTC	Current consumption	Remark
3.2 V	Typical 0.44 µA; maximum 0.7 µA	V_3V3_IN = 0 V Tamb = 25 °C
3.0 V	Typical 0.44 µA; maximum 0.7 µA	
2.1 V	Typical 0.4 µA; maximum 0.7 µA	

3.33.2 Voltage monitoring

A supervisor is provided to ensure that the module only starts after the supply voltage is within the valid range.

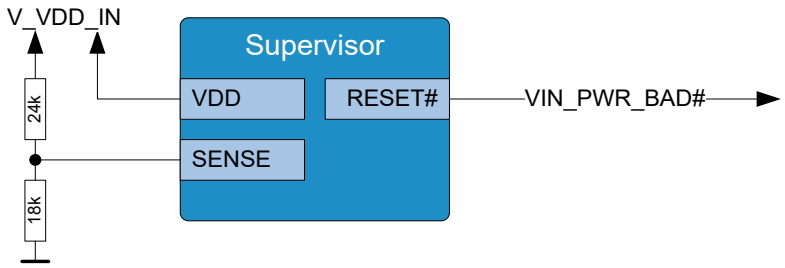


Figure 22: Block diagram supervisor

Attention: Malfunction or destruction	
	The voltage monitoring does not detect an exceedance of the maximum permitted input voltage. An excessively high supply voltage can lead to malfunctions, untimely aging or destruction of the TQMa95xxSA.

3.33.3 Power-up sequence TQMa95xxSA / carrier board

Since the TQMa95xxSA can be operated with a supply voltage of 3.0 V to 5.25 V and all voltages of the CPU signals are generated on the TQMa95xxSA, there are requirements for the mainboard design concerning the timing behavior of the voltages generated on the mainboard. The mainboard voltages are to be released exclusively by the SMARC pin CARRIER_PWRON. This is connected to the PMIC signal PGOOD.

The following figure shows the voltage regulator control of a carrier board:

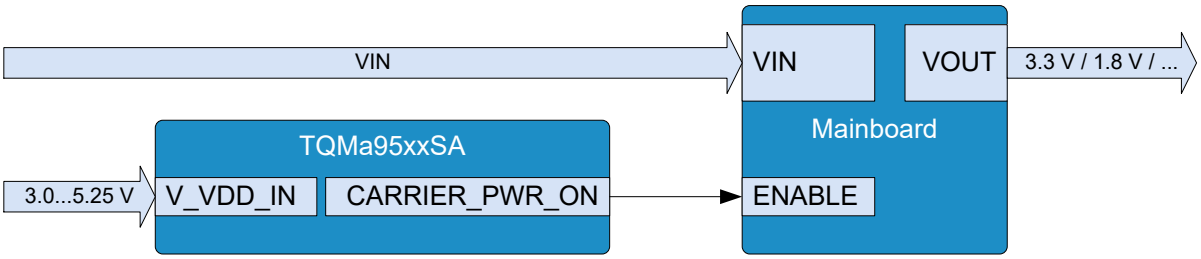


Figure 23: Block diagram power supply carrier board

Attention: Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins should be driven by external components until the power-up sequence has been completed. The mainboard voltages are to be released exclusively by the SMARC pin CARRIER_PWR_ON.

In order for the signal CARRIER_STBY# to correspond to the default from SMARC power sequencing, it is logically AND-linked to the signal CARRIER_PWR_ON. In sequencing, the rising edge at CARRIER_STBY# must not occur before the rising edge at CARRIER_PWR_ON.

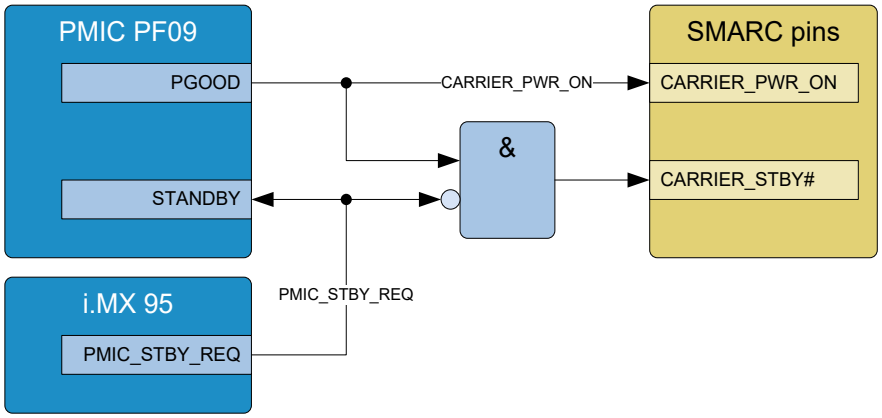


Figure 24: Block diagram CARRIER_STBY#

3.33.4 PMIC

Three PMICs are responsible for powering the i.MX 95. The PF090x is the primary PMIC that controls and monitors the other two chips and communicates with them via I2C as needed. The PF5301 and PF5302 PMICs are functionally buck regulators that provide two essential CPU voltages with low voltage but high current. The only difference is their maximum current.

The PF090x has a fixed pre-programmed power sequence in which the two PF530x are integrated. Their enable and PGOOD monitoring is done by the PF090x.

Attention: Malfunction or destruction	
	Improper PMIC programming may cause the i.MX 95 or other peripherals on the TQMa95xxSA to operate outside their specification. This can lead to malfunction, deterioration or destruction of the TQMa95xxSA.

3.34 Management Signals

The SMARC standard provides a large number of control signals. The following table shows an overview of the management signals used in accordance with the SMARC standard.

Table 13: Management signals

Signal	I/O	Level	Description	Usage
VIN_PWR_BAD#	I	VDD_IN	Status of module voltage supply from carrier	Enable signal from PMIC and buck-boost controller
CARRIER_PWR_ON	O	1.8 V	Enable signal of the power supply on carrier	PMIC PGOOD (integrated in power sequence)
CARRIER_STBY#	O	1.8 V	Standby status	PMIC_STBY_REQ from i.MX 95 to PMIC, linked with CARRIER_PWR_ON
RESET_OUT#	O	1.8 V	Reset output of PMIC	Generated from IMX_POR#; pull-up to 1.8 V
RESET_IN#	I	1.8 V	Reset input	Connected to IMX_POR# via diode; pull-up to 1.8 V
POWER_BTN#	I	1.8 V	i.MX 95 ON/OFF	i.MX 95 ON_OFF_BUTTON[2]
SLEEP#	I	1.8 V	Carrier sleep status	i.MX 95 GPIO2_IO18 (Debouncing via RC element and Schmitt Trigger)
LID#	I	1.8 V	Enclosure status	Routed to port expander (Debouncing via RC element and Schmitt Trigger)
BATLOW#	I	1.8 V	Low battery voltage	Routed to port expander
I2C_PM_DAT/CK	I/O	1.8 V	Power management I²C bus	See I²C Interfaces (3.30)
CHARGING#	I	1.8 V	Status charging	Routed to port expander
CHARGER_PRSNT#	I	1.8 V	Status charging voltage	Routed to port expander
TEST#	I	1.8 V	Test functions	NC
SMB_ALERT_1V8#	I	1.8 V	SMBus interrupt	i.MX 95 GPIO1_IO12 (Alt: SAI1_TXC))

[2] The debouncing required by the SMARC specification is omitted, as the CPU only reacts after 5 seconds.

4. MECHANICS

4.1 Connector

The TQMa95xxSA is connected to the carrier board through 314 PCB contacts.

The following table shows some suitable mating connectors for the carrier board.

Table 14: TQMa95xxSA mating connectors

Manufacturer	Part	Connector height	Board-To-Board
JAE	MM70 Series	4.3 mm, 6.7 mm	1.5 mm, 3.0 mm
Nexus Components	5242 Series	7.5 mm	5.0 mm
EFCO	30470 Series	2.7 mm, 5 mm, 11.1 mm	5.2 mm, 7.5 mm, 13.6 mm

4.2 Dimensions

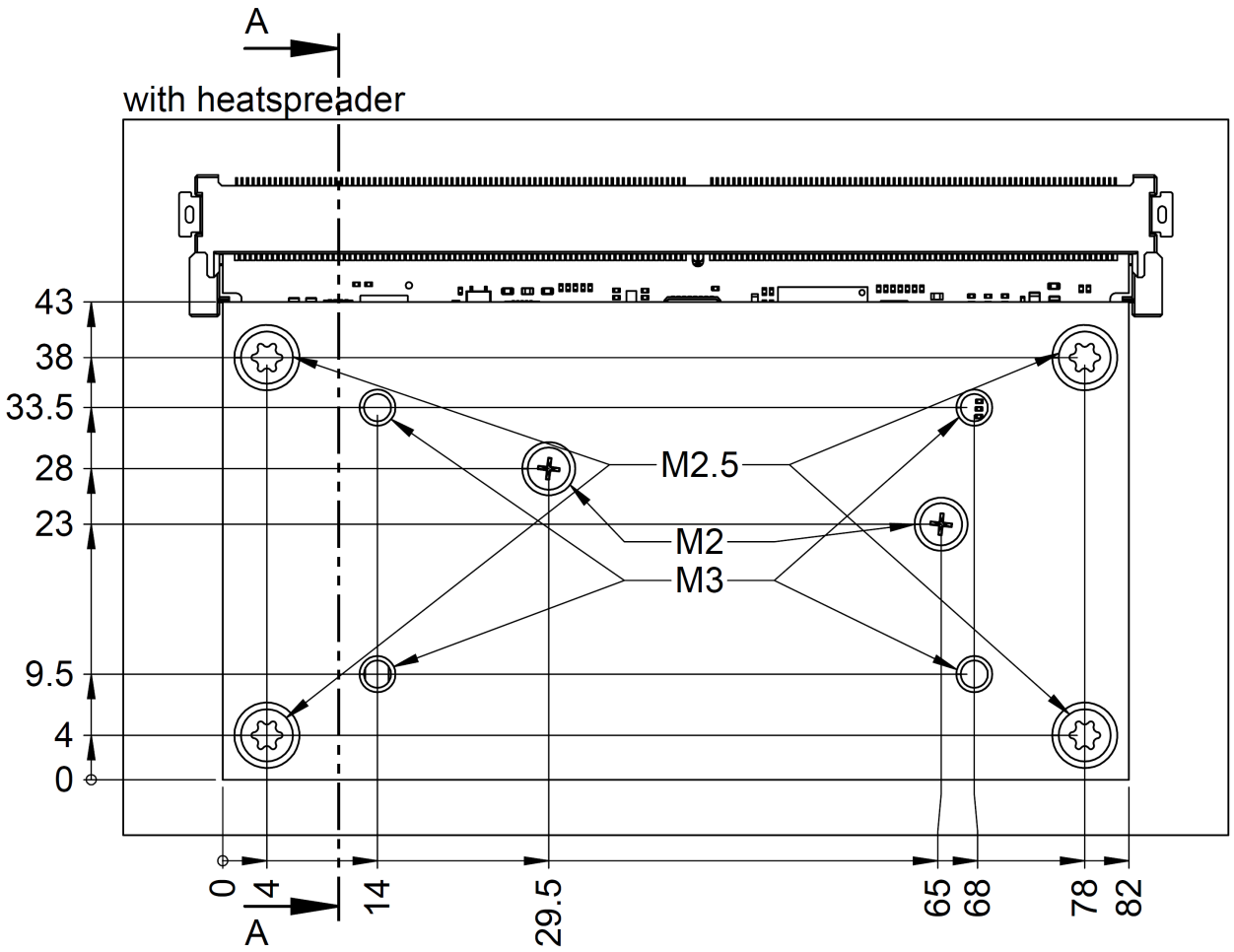


Figure 25: TQMa95xxSA dimensions

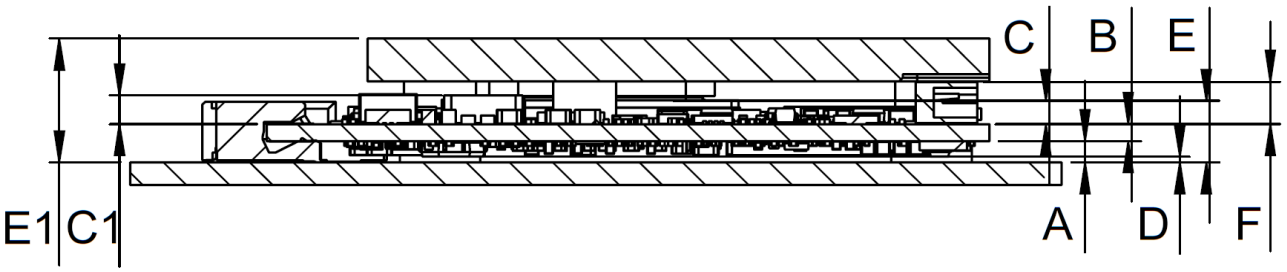


Figure 26: TQMa95xxSA heights with heatspreader

Table 15: Heights

Property	Value	Tolerance	Unit	Remark
A	1.55	±0.15	mm	Board to board distance
B	1.127	±0.113	mm	Printed circuit board thickness
C	2.10	±0.23	mm	CPU height (lidded CPU version)
C	1.56	±0.18	mm	CPU height (not lidded CPU version)
C1	1.99	±0.08	mm	Inductors height
D	0.535	±0.16	mm	Installation space under the module
E	4.78	±0.29	mm	Overall height to CPU surface - lidded CPU version
E	4.23	±0.26	mm	Overall height to CPU surface – not lidded CPU version
E1	8.75	±0.24	mm	Overall height to heatspreader
F	1.09	±0.10	mm	JTAG connector (optional) height

4.3 Component placement

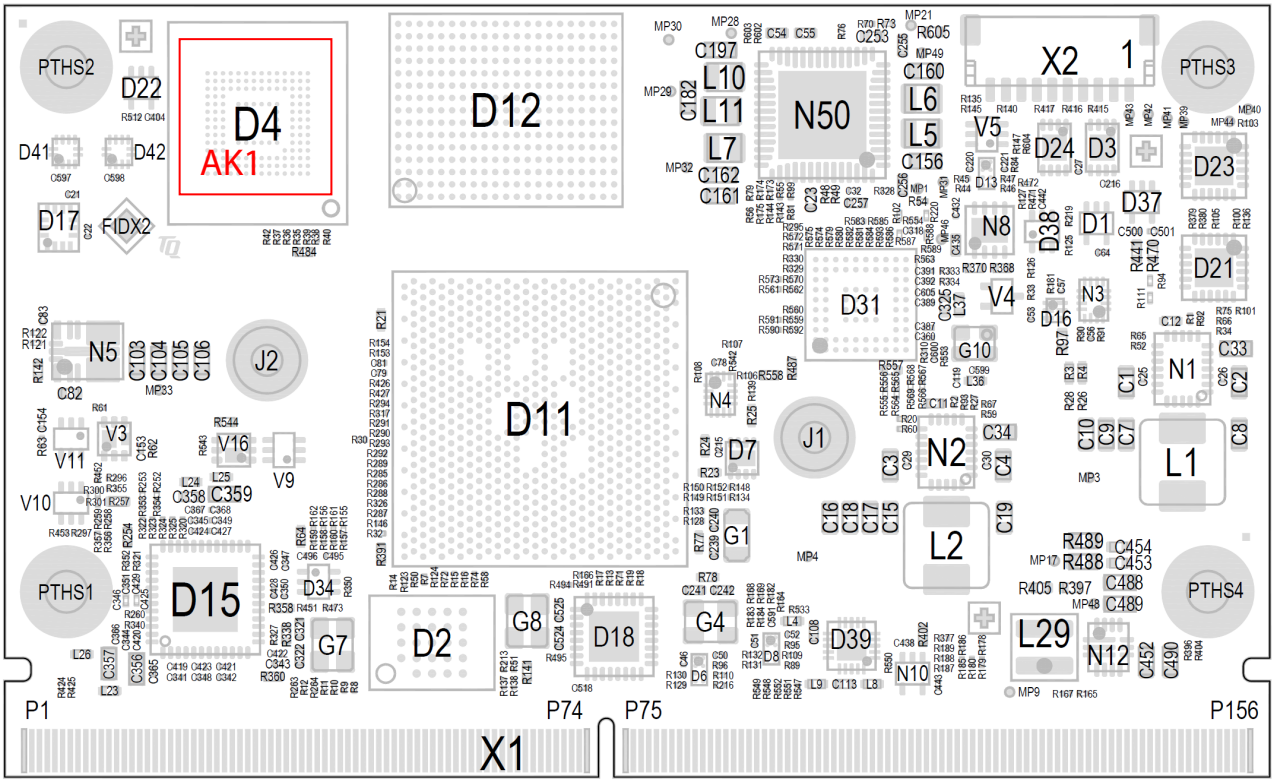


Figure 27: TQMa95xxSA, component placement top

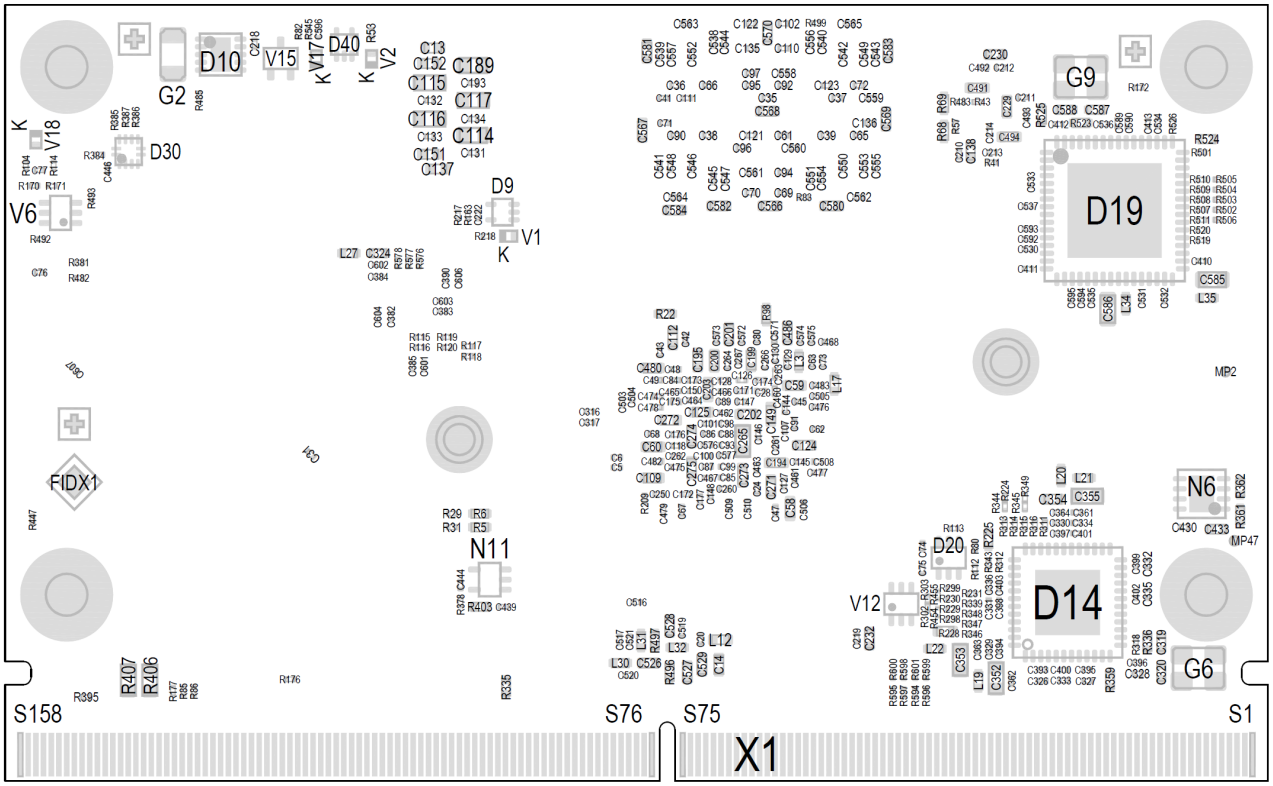


Figure 28: TQMa95xxSA, component placement bottom

The labels on the TQMa95xxSA show the following information:

Table 16: Labels on TQMa95xxSA

Label	Content
AK1	MAC address, TQMa95xxSA version and revision, serial number

4.4 Adaptation to the environment

The TQMa95xxSA has overall dimensions (length × width) of 82 mm × 50 mm (± 0,1 mm).
The TQMa95xxSA has a minimum height above the carrier board of TBD (depends on connector on carrier board).
The TQMa95xxSA weighs approximately TBD.

4.5 Protection against external effects

As an embedded module, the TQMa95xxSA is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.6 Thermal management

To cool the TQMa95xxSA, a maximum of approximately TBD watts must be dissipated, see Table TBD for peak currents.
The cooling solution must be able to dissipate this power peak; it will never occur permanently in normal operation.
The power dissipation originates primarily in the i.MX 95, the SDRAM and the PMICs.
The power dissipation also depends on the software used and can vary according to the application.
See i.MX 95 Data Sheet (1) for further information.

Attention: Destruction or malfunction, TQMa95xxSA heat dissipation	
	The TQMa95xxSA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 95 must be taken into consideration when connecting the heat sink. The i.MX 95 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa95xxSA and thus malfunction, deterioration or destruction.

4.7 Structural requirements

The TQMa95xxSA has a low retention force and has to be mounted / secured according to customer requirements.
The superior system is defined by the customer depending on the usage of the TQMa95xxSA.

5. SOFTWARE

The TQMa95xxSA is delivered with a preinstalled boot loader U-Boot and the BSP provided by TQ-Systems GmbH, which is tailored for the MB-SMARC-2.
The boot loader U-Boot provides TQMa95xxSA-specific as well as board-specific settings, e.g.:

- i.MX 95 configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader is used.
More information can be found in the TQ-Support Wiki for the TQMa95xxSA.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa95xxSA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs for multi-pole interfaces (e.g. LC display).

As part of the development, an EMC test was performed with the starter kit MB-SMARC-2 REV.02xx in accordance with EN55022:2010 Class A limits.

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures are provided on the TQMa95xxSA.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Climate and operational conditions

The operating temperature range for the TQMa95xxSA strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa95xxSA.
The TQMa95xxSA is available in three different variants with different temperature ranges. In general, a reliable operation is given when following conditions are met:

Table 17: Climate and operational conditions industrial temperature range

Parameter	Range	Remark
Ambient temperature	–25 °C to +85 °C	–
Extended temperature	–40 °C to +85 °C	–
Storage temperature	-40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Attention: Destruction or malfunction, TQMa95xxSA heat dissipation	
	The TQMa95xxSA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 95 must be taken into consideration when connecting the heat sink. The i.MX 95 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa95xxSA and thus malfunction, deterioration or destruction.

6.5 Reliability and service life

The calculated MTBF of the TQMa95xxSA is approximately 495787 h @ +40 °C ambient temperature, Ground, Benign.
The TQMa95xxSA is designed to be insensitive to shock and vibration.

6.6 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa95xxSA is only a sub-component of an overall system.

6.7 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship, irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.8 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.
The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa95xxSA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa95xxSA was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.
The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.
Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.
TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

7.5 EuP

The Eco Design Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa95xxSA must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the TQMa95xxSA enable compliance with EuP requirements for the TQMa95xxSA.

7.6 Battery

No batteries are assembled on the TQMa95xxSA.

7.7 Packaging

The TQMa95xxSA is delivered in reusable packaging.

7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa95xxSA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa95xxSA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)

- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 18: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
ASIL	Automotive Safety Integrity Level
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR	Double Data Rate
DNC	Do Not Connect
DP	DisplayPort
DSI	Display Serial Interface
ECC	Error-Correcting Code
eDP	embedded DisplayPort
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card
ESD	Electrostatic Discharge
eSPI	enhanced Serial Peripheral Interface
EU	European Union
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General-Purpose Input/Output
GPMC	General-Purpose Memory Controller
GPO	General-Purpose Output
GPU	Graphics Processing Unit
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IC	Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LVDS	Low-Voltage Differential Signalling
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MIPI	Mobile Industry Processor Interface
MMC	Multimedia Card
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTBF	Mean (operating) Time Between Failures

8.1 Acronyms and definitions (continued)

Table 18: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NOR	Not-Or
OD	Open-drain
OTG	On-The-Go
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
R/W	Read/Write
RAM	Random Access Memory
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protected
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDIO	Secure Digital Input/Output
SDRAM	Synchronous Dynamic Random Access Memory
SMARC	Smart Mobile ARChitecture
SMBus	System Management Bus
SPI	Serial Peripheral Interface
TBD	To Be Determined
TSE	Trust Secure Element
UART	Universal Asynchronous Receiver / Transmitter
UM	User's Manual
USB	Universal Serial Bus
VPU	Video Processing Unit
WDT	Watchdog Timer
WEEE®	Waste Electrical and Electronic Equipment
WP	Write Protect

8.2 References

Table 19: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 95 Industrial Application Processors Data Sheet	Ref.1 Draft F, 06/2023	NXP
(2)	i.MX 95 Applications Processor ReferenceManual	Rev. 1, 02/2024	NXP
(3)	i.MX 95 Mask Set Errata	Rev. A, 01/2024	NXP
(4)	PF09 - 9-channel Power Management IC	Rev. 0.4, 08.2023	NXP
(5)	i.MX 95 Hardware Developer's Guide	Rev. A, 11/2023	NXP
(6)	SMARC Hardware Specification V2.1.1	Version 2.1.1, 20.05.2020	SGET
(7)	MB-SMARC-2 User's Manual	– current –	TQ-Systems
(8)	TQMa95xxSA Support-Wiki	– current –	TQ-Systems

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