MBa95xxCA
Preliminary User's Manual

MBa95xxCA UM 0001
21.01.2025

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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	21.01.2025	Kreuzer		First edition

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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa95xxCA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa95xxCA schematics
- TQMa95xxLA User's Manual
- i.MX 95 Data Sheet
- i.MX 95 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa95xxLA

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of the MBa95xxCA as of revision 01xx. The MBa95xxCA is designed as a carrier board for the TQ-Minimodul TQMa95xxLA on the adapter TQMa95xxLA-ADAP.

Core of the MBa95xxCA is the TQMa95xxLA with an NXP i.MX 95 CPU.

The TQMa95xxLA connects all peripheral components. In addition to the standard communication interfaces such as USB, Ethernet, etc., all other available signals of the TQMa95xxLA are routed on 100 mil standard pin headers on the MBa95xxCA.

CPU features and interfaces can be evaluated, software development for a TQMa95xxLA based project can start immediately.

2.1 MBa95xxCA block diagram

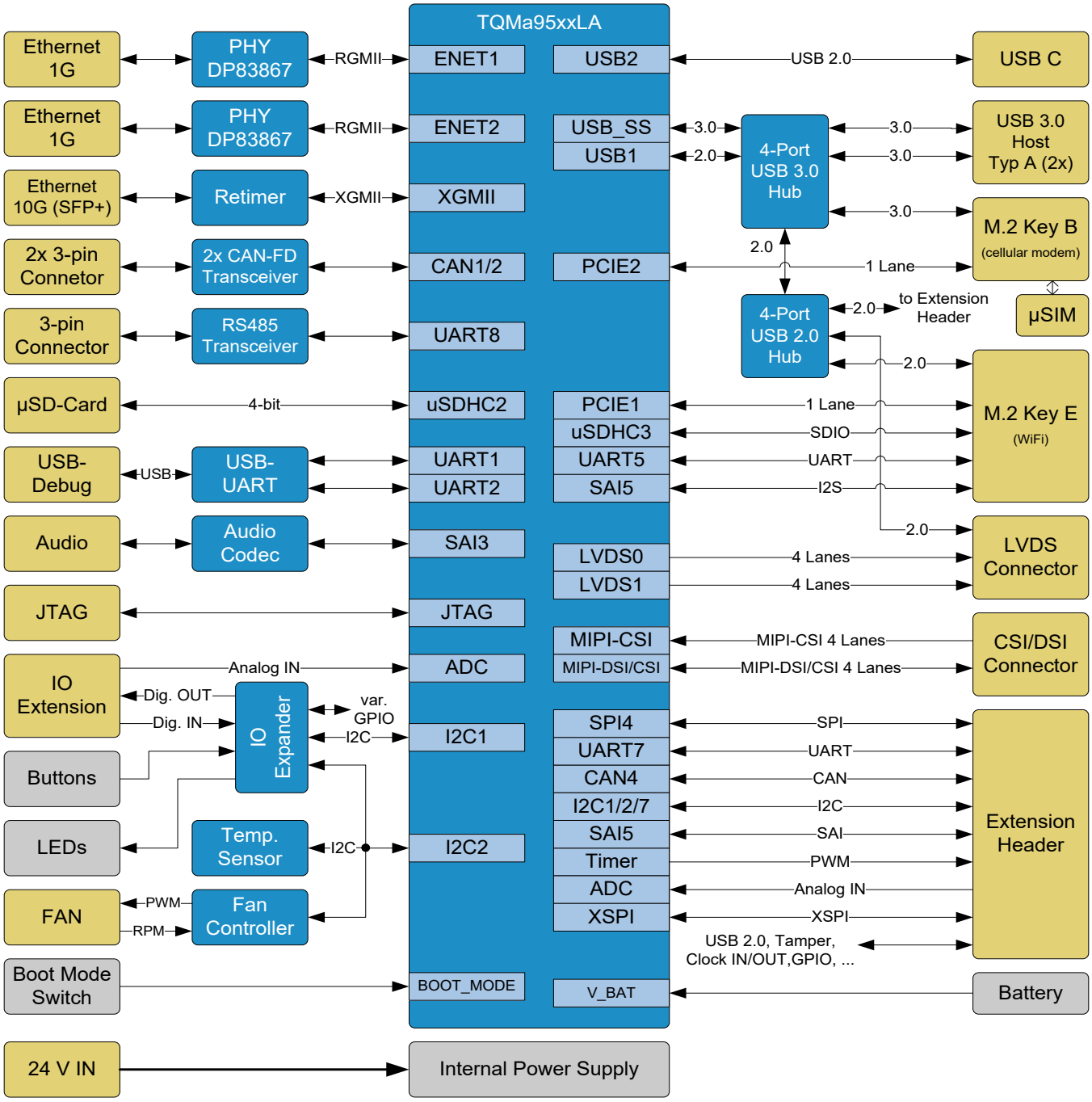


Figure 1: Block diagram MBa95xxCA

2.2 MBa95xxCA data interfaces

The following interfaces/functions and user interfaces are available on the MBa95xxCA:

Table 2: Data interfaces & power connectors

Interface	Connector	Type
Audio	X22, X23, X24	Audio Jack, 3.5 mm
CAN-FD	X13, X14	3-pin Phoenix
Coin cell	X34	CR2032 holder
Ethernet, 1000 Base-T	X10, X11	RJ-45, integrated magnetics
Ethernet, 10G / SFP+	X12 + X35	20-pin SFP connector + cage
Extension headers	X4, X5, X6	100 mil header, 2 × 40-pin, 1 x 10-pin
External battery	X32	2-pin header
Fan	X30	4-pin header
IO (digital / analog)	X25	30-pin terminal block
ISO 14443	X33	2-pin header for antenna
LVDS	X19	30-pin, DF19G
LVDS CMD	X20	20-pin, DF19G
M.2	X16	M.2 Socket Key E
	X17	M.2 Socket Key B
	X18	Micro-SIM card holder
MIPI-DSI/CSI	X21	60-pin, Board-to-Board
Power In	X28	DC jack (2.5 mm / 5.5 mm)
	X29	2-pin screw terminal block
RS485	X15	3-pin Phoenix
SD card, UHS-I	X7	Push-Pull
USB 3.0 Host	X8	USB, stacked Type A
USB Type C	X9	USB, Type C
USB debug	X26	USB, Micro AB

The MBa95xxCA provides the following diagnostic and user interfaces:

Table 3: Diagnostic and user interfaces

Interface	Component	Remark
Status LEDs	7 × green LED	Power LEDs
	5 × green LED	4 × USB Host, 1 × USB Type-C
	1 × green LED	Debug LED for USB debug interface
	1 × green LED	User LED1
	1 × orange LED	User LED2
	3 × green LED	M.2
	1 × red LED	Reset LED
	2 × green / 2 x yellow LED	Ethernet LEDs (Activity / Speed)
	1 x green LED	SD card
Temperature sensor	1 × SE97BTP	Digital I^2C temperature sensor
Power / Reset button	2 × Push button	ONOFF, RESET
General Purpose button	2 × Push button	GP push button at port expander
Boot Mode configuration	1 × 4-fold DIP switch	Boot Mode configuration
CAN termination	2 × 2-fold DIP switch	S6, S7
JTAG	1 × 10-pin, 100 mil header	X27
RS485 termination	1 x 2-fold DIP switch	S8

3. ELECTRONICS

The following chapters describe the interfaces of the MBa95xxCA as of revision 01xx in connection with a TQMa95xxLA with maximum configuration. In any case the TQMa95xxLA User's Manual must be complied with.

3.1 TQMa95xxLA

The TQMa95xxLA is the central system on the MBa95xxCA. It provides LPDDR5 SDRAM, eMMC, temperature sensor with EEPROM, power supply and power management functionality. Further functionalities are optionally available (see Figure 2).

All TQMa95xxLA internal voltages are derived from the 5 V supply voltage. All functionally relevant pins of the CPU are routed to the TQMa95xxLA pads. This enables the user to use the TQMa95xxLA with all the freedom that comes with a customer-specific design-in solution. Further information can be found in the TQMa95xxLA User's Manual.

On the MBa95xxCA the standard interfaces like USB, Ethernet, etc., provided by the TQMa95xxLA are routed to industry standard connectors. All other signals and buses provided by the TQMa95xxLA are routed to 100 mil headers. The boot behaviour of the TQMa95xxLA can be configured. The Boot Mode configuration is set by a DIP switch on the MBa95xxCA, see chapter 3.2.

Furthermore, the MBa95xxCA provides all power supplies and configurations required for the operation of the TQMa95xxLA.

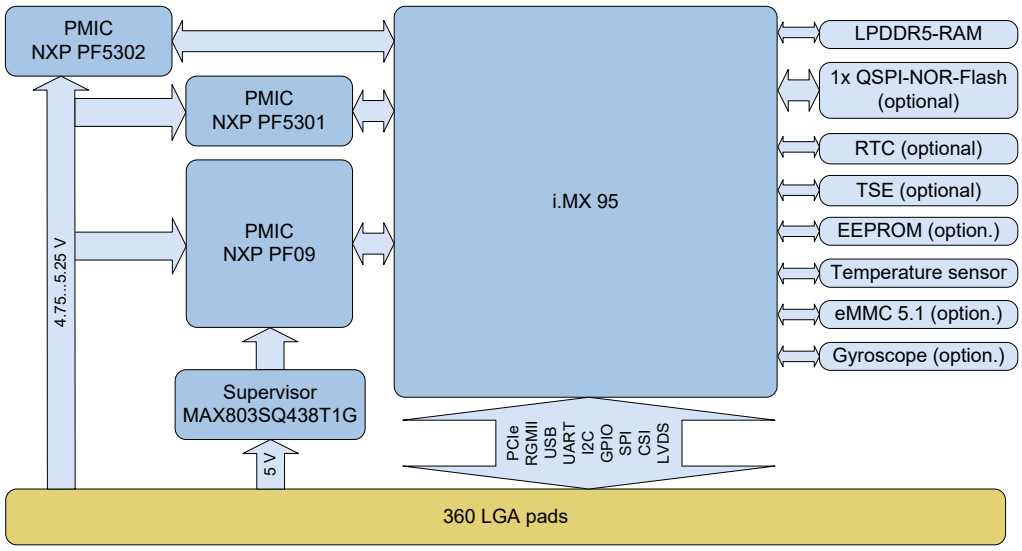


Figure 2: Block diagram TQMa95xxLA

3.1.1 TQMa95xxLA-ADAP connectors on MBa95xxCA

The TQMa95xxLA is connected via the adapter TQMa95xxLA-ADAP to the MBa95xxCA with 360 pins on three connectors (2 x EPT 401-51301-51, 1 x EPT 401-51701-51). Connector samples are available from: https://www.ept.de/index.php?tq-colibri-lp

3.1.2 MBa95xxCA/TQMa95xxLA-ADAP pinout

All available TQMa95xxLA signals are accessible on the three connectors X1, X2, and X3 of the MBa95xxCA.

The pins assignment listed in Table 4, Table 5, and Table 6 refer to the corresponding BSP provided by TQ-Systems.

Further information such as pull-ups or pull-downs on the TQMa95xxLA can be found in the TQMa95xxLA User's Manual (6).

For information regarding I/O pins in Table 4, Table 5, and Table 6 refer to the i.MX 95 documentation see Table 40.

3.1.2 MBa95xxCA/TQMa95xxLA-ADAP pinout (continued)

Table 4: Pinout connector X1

Board signal	Module signal	Pin number		Module signal	Board signal
ETH_CLK_P	ETH_CLK_P	A1	B1	JTAG_TMS	JTAG_TMS
ETH_CLK_N	ETH_CLK_N	A2	B2	JTAG_TCK	JTAG_TCK
GND	GND	A3	B3	GND	GND
ETH_TX_P	ETH_TX_P	A4	B4	JTAG_TDI	JTAG_TDI
ETH_TX_N	ETH_TX_N	A5	B5	JTAG_TDO	JTAG_TDO
GND(FIXED)	GND(FIXED)	A6	B6	GND(FIXED)	GND(FIXED)
ETH_RX_P	ETH_RX_P	A7	B7	CLKO1	M2_KEYE_SUSCLK
ETH_RX_N	ETH_RX_N	A8	B8	CLKO2	M2_KEYB_SUSCLK
GND	GND	A9	B9	GND	GND
ENET2_TXD0	ENET1_TXD0	A10	B10	CLKO3	CAM0_MCLK[1]
ENET2_TXD1	ENET1_TXD1	A11	B11	CLKO4	CAM1_MCLK[2]
ENET2_TXD2	ENET1_TXD2	A12	B12	GND	GND
ENET2_TXD3	ENET1_TXD3	A13	B13	RTC_INT#	RTC_EVENT_MOD#
GND	GND	A14	B14	TEMP_EVENT#	TEMP_EVENT_MOD#
ENET2_TXC	ENET1_TXC	A15	B15	RESET_OUT#	RESET_OUT#
GND(FIXED)	GND(FIXED)	A16	B16	GND(FIXED)	GND(FIXED)
ENET2_TX_CTL	ENET1_TX_CTL	A17	B17	RESET_IN#	RESET_IN#
ENET2_RX_CTL	ENET1_RX_CTL	A18	B18	PMIC_ON_REQ	PMIC_ON_REQ
GND	GND	A19	B19	GND	GND
ENET2_RXD0	ENET1_RXD0	A20	B20	PGOOD	PGOOD
ENET2_RXD1	ENET1_RXD1	A21	B21	WDOG_ANY	WDOG_ANY
ENET2_RXD2	ENET1_RXD2	A22	B22	IMX_ONOFF#	IMX_ONOFF#
ENET2_RXD3	ENET1_RXD3	A23	B23	GND	GND
GND	GND	A24	B24	GPIO2_IO16	SAI3_TX_BCLK
ENET2_RXC	ENET1_RXC	A25	B25	GPIO2_IO17	SAI3_MCLK
GND(FIXED)	GND(FIXED)	A26	B26	GND(FIXED)	GND(FIXED)
ENET1_MDIO	ENET1_MDIO	A27	B27	GPIO2_IO18	LCD_PWM
ENET1_MDC	ENET1_MDC	A28	B28	GPIO2_IO19	SPI4_SIN
GND	GND	A29	B29	GND	GND
FS0B	FS0B	A30	B30	GPIO2_IO20	SAI3_RXD0
AMUX	AMUX	A31	B31	GPIO2_IO21	SAI3_TXD0
GND	GND	A32	B32	GND	GND
GND	GND	A33	B33	UART1_TX	BM0_UART1_TX
V_3V3_SD	V_3V3_SD	A34	B34	UART1_RX	UART1_RX
V_3V3	V_3V3	A35	B35	GND	GND
GND(FIXED)	GND(FIXED)	A36	B36	GND(FIXED)	GND(FIXED)
V_5V_TQM	V_5V_IN	A37	B37	GND	GND
V_5V_TQM	V_5V_IN	A38	B38	V_5V_IN	V_5V_TQM
V_5V_TQM	V_5V_IN	A39	B39	V_5V_IN	V_5V_TQM
GND	GND	A40	B40	GND	GND
GND	GND	A41	B41	GND	GND
V_5V_TQM	V_5V_IN	A42	B42	V_5V_IN	V_5V_TQM
V_5V_TQM	V_5V_IN	A43	B43	V_5V_IN	V_5V_TQM
V_5V_TQM	V_5V_IN	A44	B44	GND	GND
GND(FIXED)	GND(FIXED)	A45	B45	GND(FIXED)	GND(FIXED)
V_SD	V_SD2	A46	B46	GPIO2_IO22	GYRO_INT2_MOD
V_1V8_MOD	V_1V8	A47	B47	GPIO2_IO23	M2_KEYE_ALERT#
GND	GND	A48	B48	GPIO2_IO24	HEADER_PWM
GND	GND	A49	B49	GPIO2_IO25	CAN2_TX
RFU	RFU	A50	B50	GPIO2_IO26	SAI3_TX_SYNC
GND	GND	A51	B51	GPIO2_IO27	CAN2_RX
ENET1_TX_CTL	ENET0_TX_CTL	A52	B52	GND	GND
GND	GND	A53	B53	GPIO2_IO03	UART5_RTS#
ENET1_TXC	ENET0_TXC	A54	B54	GPIO2_IO02	UART5_CTS#
GND(FIXED)	GND(FIXED)	A55	B55	GND(FIXED)	GND(FIXED)
ENET1_TXD0	ENET0_TXD0	A56	B56	GPIO2_IO01	UART5_RX
ENET1_TXD1	ENET0_TXD1	A57	B57	GPIO2_IO00	UART5_TX
ENET1_TXD2	ENET0_TXD2	A58	B58	GND	GND
ENET1_TXD3	ENET0_TXD3	A59	B59	GPIO2_IO28	USB_C_ALERT#
GND	GND	A60	B60	GPIO2_IO29	10G_RET_LOSS
ENET1_RXD0	ENET0_RXD0	A61	B61	GPIO2_IO30	SFP_TX_FAULT
ENET1_RXD1	ENET0_RXD1	A62	B62	GPIO2_IO31	SFP_RX_LOSS
ENET1_RXD2	ENET0_RXD2	A63	B63	GND	GND
ENET1_RXD3	ENET0_RXD3	A64	B64	GPIO2_IO15	UART8_RTS#
GND(FIXED)	GND(FIXED)	A65	B65	GND(FIXED)	GND(FIXED)
ENET1_RX_CTL	ENET0_RX_CTL	A66	B66	GPIO2_IO14	PEX2_INT#
GND	GND	A67	B67	GPIO2_IO13	UART8_RX
ENET1_RXC	ENET0_RXC	A68	B68	GPIO2_IO12	UART8_TX
GND	GND	A69	B69	GND	GND
ENET2_INT#	ENET0_MDC	A70	B70	SD2_RESET#	SD2_RESET#
USB1_OTG_PWR	ENET0_MDIO	A71	B71	SD2_CD#	SD2_CD#
GND	GND	A72	B72	GND	GND
SD3_CMD	SD3_CMD	A73	B73	SD2_CMD	SD2_CMD
SD3_CLK	SD3_CLK	A74	B74	SD2_CLK	SD2_CLK
GND(FIXED)	GND(FIXED)	A75	B75	GND(FIXED)	GND(FIXED)
SD3_DATA3	SD3_DATA3	A76	B76	SD2_DATA3	SD2_DATA3
SD3_DATA2	SD3_DATA2	A77	B77	SD2_DATA2	SD2_DATA2
GND	GND	A78	B78	GND	GND
SD3_DATA1	SD3_DATA1	A79	B79	SD2_DATA1	SD2_DATA1
SD3_DATA0	SD3_DATA0	A80	B80	SD2_DATA0	SD2_DATA0

[1] Can be changed to CCM_CLKO3 by placing R529 and removing R530
[2] Can be changed to CCM_CLKO4 by placing R532 and removing R531

3.1.2 MBa95xxCA/TQMa95xxLA-ADAP pinout (continued)

Table 5: Pinout connector X2

Board signal	Module signal	Pin number		Module signal	Board signal
ADC_IN0	ADC_IN0	A1	B1	LVDS0_D3_P	LVDS0_D3_P
ADC_IN1	ADC_IN1	A2	B2	LVDS0_D3_N	LVDS0_D3_N
GND	GND	A3	B3	GND	GND
ADC_IN2	ADC_IN2	A4	B4	LVDS0_CLK_P	LVDS0_CLK_P
ADC_IN3	ADC_IN3	A5	B5	LVDS0_CLK_N	LVDS0_CLK_N
GND(FIXED)	GND(FIXED)	A6	B6	GND(FIXED)	GND(FIXED)
ADC_IN4	ADC_IN4	A7	B7	LVDS0_D2_P	LVDS0_D2_P
ADC_IN5	ADC_IN5	A8	B8	LVDS0_D2_N	LVDS0_D2_N
GND	GND	A9	B9	GND	GND
ADC_IN6	ADC_IN6	A10	B10	LVDS0_D1_P	LVDS0_D1_P
ADC_IN7	ADC_IN7	A11	B11	LVDS0_D1_N	LVDS0_D1_N
GND	GND	A12	B12	GND	GND
TSE_ISO_7816_IO1	TSE_ISO_7816_IO1	A13	B13	LVDS0_D0_P	LVDS0_D0_P
TSE_ISO_7816_IO2	TSE_ISO_7816_IO2	A14	B14	LVDS0_D0_N	LVDS0_D0_N
TSE_ISO_7816_CLK	TSE_ISO_7816_CLK	A15	B15	GYRO_INT1	GYRO_INT1_MOD
GND(FIXED)	GND(FIXED)	A16	B16	GND(FIXED)	GND(FIXED)
TSE_ISO_7816_RST#	TSE_ISO_7816_RST#	A17	B17	GYRO_INT2	GYRO_INT2_MOD
GND	GND	A18	B18	LVDS1_D3_P	LVDS1_D3_P
XSPI_SCLK[1]	XSPI_SCLK	A19	B19	LVDS1_D3_N	LVDS1_D3_N
GND	GND	A20	B20	GND	GND
XSPI_SS0#[1]	XSPI_SS0#	A21	B21	LVDS1_CLK_P	LVDS1_CLK_P
XSPI_DATA0[1]	XSPI_DATA0	A22	B22	LVDS1_CLK_N	LVDS1_CLK_N
XSPI_DATA1[1]	XSPI_DATA1	A23	B23	GND	GND
XSPI_DATA2[1]	XSPI_DATA2	A24	B24	LVDS1_D2_P	LVDS1_D2_P
XSPI_DATA3[1]	XSPI_DATA3	A25	B25	LVDS1_D2_N	LVDS1_D2_N
GND(FIXED)	GND(FIXED)	A26	B26	GND(FIXED)	GND(FIXED)
SAI5_TXD0	XSPI_DATA4	A27	B27	LVDS1_D1_P	LVDS1_D1_P
SAI5_TX_SYNC	XSPI_DATA5	A28	B28	LVDS1_D1_N	LVDS1_D1_N
SAI5_TX_BCLK	XSPI_DATA6	A29	B29	GND	GND
SAI5_RXD0	XSPI_DATA7	A30	B30	LVDS1_D0_P	LVDS1_D0_P
GND	GND	A31	B31	LVDS1_D0_N	LVDS1_D0_N
SAI5_RX_BCLK	XSPI_SS1#	A32	B32	GND	GND
SAI5_RX_SYNC	XSPI_DQS	A33	B33	GND	GND
GND	GND	A34	B34	USB1_SS_RX1_P	USB1_SS_RX1_P
V_3V3_MOD	V_GPIO	A35	B35	USB1_SS_RX1_N	USB1_SS_RX1_N
GND(FIXED)	GND(FIXED)	A36	B36	GND(FIXED)	GND(FIXED)
BM2_RTC_EVENT_MOD#	SAI1_TXFS	A37	B37	USB1_SS_TX1_P	USB1_SS_TX1_P
BM3_CAN1_TX	SAI1_TXD0	A38	B38	USB1_SS_TX1_N	USB1_SS_TX1_N
GND	GND	A39	B39	GND	GND
CAN1_RX	SAI1_TXC	A40	B40	USB1_D_P	USB1_D_P
PEX1_INT#	SAI1_RXD0	A41	B41	USB1_D_N	USB1_D_N
GND	GND	A42	B42	GND	GND
UART2_RX	UART2_RX	A43	B43	USB1_SS_RX0_P	USB1_SS_RX0_P
BM1_UART2_TX	UART2_TX	A44	B44	USB1_SS_RX0_N	USB1_SS_RX0_N
GND(FIXED)	GND(FIXED)	A45	B45	GND(FIXED)	GND(FIXED)
I2C1_SDA	I2C1_SDA	A46	B46	USB1_SS_TX0_P	USB1_SS_TX0_P
I2C1_SCL	I2C1_SCL	A47	B47	USB1_SS_TX0_N	USB1_SS_TX0_N
GND	GND	A48	B48	GND	GND
I2C2_SDA	I2C2_SDA	A49	B49	USB1_VBUS	USB1_VBUS_DET
I2C2_SCL	I2C2_SCL	A50	B50	USB2_VBUS	USB2_VBUS_DET
GND	GND	A51	B51	USB2_ID	USB2_ID
I2CX_SDA	I2CX_SDA	A52	B52	GND	GND
I2CX_SCL	I2CX_SCL	A53	B53	USB2_D_P	USB2_D_P
GND	GND	A54	B54	USB2_D_N	USB2_D_N
GND(FIXED)	GND(FIXED)	A55	B55	GND(FIXED)	GND(FIXED)
TSE_ISO_14443_LA	TSE_ISO_14443_LA	A56	B56	CLK_IN2	CLK_IN2
TSE_ISO_14443_LB	TSE_ISO_14443_LB	A57	B57	GND	GND
GND	GND	A58	B58	CLK_IN1	CLK_IN1
EARC_N_HPD	EARC_N_HPD	A59	B59	GND	GND
EARC_P_UTIL	EARC_P_UTIL	A60	B60	PCIE_REF_OUT_CLK_P	PCIE_REF_OUT_CLK_P
GND	GND	A61	B61	PCIE_REF_OUT_CLK_N	PCIE_REF_OUT_CLK_N
EARC_AUX	EARC_AUX	A62	B62	GND	GND
GND	GND	A63	B63	PCIE1_REFCLK_P	PCIE1_REFCLK_P
V_BAT	V_BAT	A64	B64	PCIE1_REFCLK_N	PCIE1_REFCLK_N
GND(FIXED)	GND(FIXED)	A65	B65	GND(FIXED)	GND(FIXED)
SPI4_SCLK	GPIO2_IO37	A66	B66	PCIE1_RX_P	PCIE1_RX_P
SPI4_SOUT	GPIO2_IO36	A67	B67	PCIE1_RX_N	PCIE1_RX_N
GND	GND	A68	B68	GND	GND
PCIE2_CLKREQ_CPU#	GPIO2_IO35	A69	B69	PCIE1_TX_P	PCIE1_TX_P
SPI4_PCS0#	GPIO2_IO34	A70	B70	PCIE1_TX_N	PCIE1_TX_N
GND	GND	A71	B71	GND	GND
SPI4_PCS1#	GPIO2_IO33	A72	B72	GND	GND
PCIE1_CLKREQ_CPU#	GPIO2_IO32	A73	B73	PCIE2_REFCLK_P	PCIE2_REFCLK_P
GND	GND	A74	B74	PCIE2_REFCLK_N	PCIE2_REFCLK_N
GND(FIXED)	GND(FIXED)	A75	B75	GND(FIXED)	GND(FIXED)
UART7_TX	GPIO2_IO08	A76	B76	PCIE2_RX_P	PCIE2_RX_P
UART7_RX	GPIO2_IO09	A77	B77	PCIE2_RX_N	PCIE2_RX_N
GND	GND	A78	B78	GND	GND
UART7_CTS#	GPIO2_IO10	A79	B79	PCIE2_TX_P	PCIE2_TX_P
UART7_RTS#	GPIO2_IO11	A80	B80	PCIE2_TX_N	PCIE2_TX_N

[1] Disabled (default) by not placing R545 to R553

3.1.2 MBa95xxCA/TQMa95xxLA-ADAP pinout (continued)

Table 6: Pinout connector X3

Board signal	Module signal	Pin number		Module signal	Board signal
MIPI_CSI1_D3_P	MIPI_CSI1_D3_P	A1	B1	MIPI_DSICSI1_D3_P	MIPI_DSICSI1_D3_P
MIPI_CSI1_D3_N	MIPI_CSI1_D3_N	A2	B2	MIPI_DSICSI1_D3_N	MIPI_DSICSI1_D3_N
GND	GND	A3	B3	GND	GND
MIPI_CSI1_D2_P	MIPI_CSI1_D2_P	A4	B4	MIPI_DSICSI1_D2_P	MIPI_DSICSI1_D2_P
MIPI_CSI1_D2_N	MIPI_CSI1_D2_N	A5	B5	MIPI_DSICSI1_D2_N	MIPI_DSICSI1_D2_N
GND(FIXED)	GND(FIXED)	A6	B6	GND(FIXED)	GND(FIXED)
MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P	A7	B7	MIPI_DSICSI1_CLK_P	MIPI_DSICSI1_CLK_P
MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N	A8	B8	MIPI_DSICSI1_CLK_N	MIPI_DSICSI1_CLK_N
GND	GND	A9	B9	GND	GND
MIPI_CSI1_D1_P	MIPI_CSI1_D1_P	A10	B10	MIPI_DSICSI1_D1_P	MIPI_DSICSI1_D1_P
MIPI_CSI1_D1_N	MIPI_CSI1_D1_N	A11	B11	MIPI_DSICSI1_D1_N	MIPI_DSICSI1_D1_N
GND	GND	A12	B12	GND	GND
MIPI_CSI1_D0_P	MIPI_CSI1_D0_P	A13	B13	MIPI_DSICSI1_D0_P	MIPI_DSICSI1_D0_P
MIPI_CSI1_D0_N	MIPI_CSI1_D0_N	A14	B14	MIPI_DSICSI1_D0_N	MIPI_DSICSI1_D0_N
GND(FIXED)	GND(FIXED)	A15	B15	GND(FIXED)	GND(FIXED)
I2C7_SCL	GPIO2_IO07	A16	B16	GPIO2_IO05	CAN4_RX
I2C7_SDA	GPIO2_IO06	A17	B17	GPIO2_IO04	CAN4_TX
GND	GND	A18	B18	GND	GND
M33_NMI	PDM_BIT1	A19	B19	TAMPER1	TAMPER1
ENET1_INT#	PDM_BIT0	A20	B20	TAMPER0	TAMPER0

3.2 Boot Mode configuration

The TQMa95xxLA can boot from different boot sources. The boot source is selected on the MBa95xxCA via DIP switches (S1). The following table shows the possible boot configurations of the i.MX95, where Serial NAND is not supported by the MBa95xxCA.

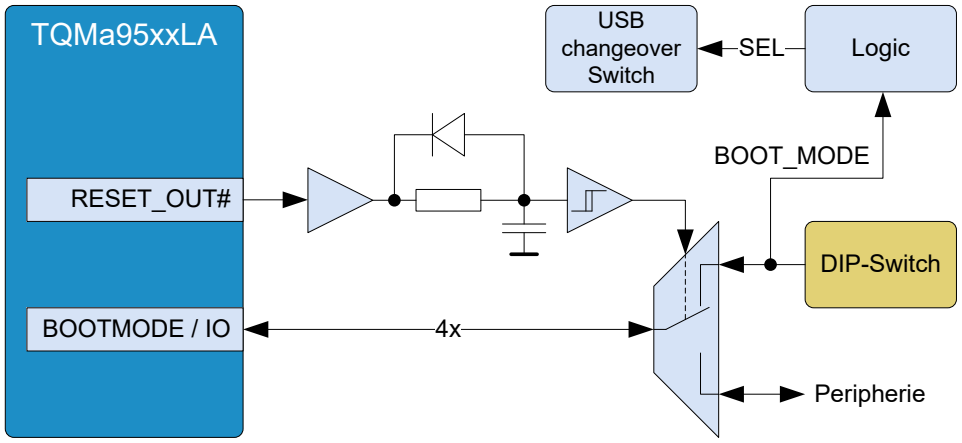


Figure 3: Block diagram boot mode

The four BOOT_MODE pins of the CPU are not dedicated pins, but are multiplexed with functional IO pins. So that neither connected periphery influences the boot mode nor the boot configuration influences the connected periphery, the pins are switched via analog switch. The RESET_OUT# signal is used for toggling, which triggers the switch with a delay (approx. 5 ms) after RESET_OUT# has been released by the logic and RC element. The switch back to the DIP switch is done almost without delay at a low edge at RESET_OUT#.

At the BOOT_MODE signals 100 kΩ pull-down resistors are provided. The 3.3 V provided by the module are used as pull-up voltage for the switchable 4.7 kΩ resistors.

The BOOT_MODE signals are also used for the logic to switch from the USB1 interface to the USB Type-C interface.

Table 7: Boot Mode configuration

Boot-Mode	S1-4 (BM3)		S1-3 (BM2)		S1-2 (BM1)		S1-1 (BM0)		Remark
	Pos.	Level	Pos.	Level	Pos.	Level	Pos.	Level	
Boot from eFuses	OFF	0	OFF	0	OFF	0	OFF	0	–
Serial Downloader (USB 1)	OFF	0	OFF	0	OFF	0	ON	1	–
eMMC (USDCH1)	OFF	0	OFF	0	ON	1	OFF	0	–
SD card (USDHC2)	OFF	0	OFF	0	ON	1	ON	1	–
FlexSPI Serial NOR	OFF	0	ON	1	OFF	0	OFF	0	–

Note: Boot from NAND	
	Booting from NAND is not supported on the MBa95xxCA.

3.3 I²C devices

Due to the large number of I2C devices on the TQMa95xxLA, special attention must be paid to the I2C1 and I2C2 addresses already in use. Depending on the application and software load the number of used I2C devices may limit the data throughput or block the bus.

Table 8: I²C signals

Signal	MBa95xxCA pin
I2C1_SDA	X2-A46
I2C1_SCL	X2-A47
I2C2_SDA	X2-A49
I2C2_SCL	X2-A50
I2C7_SDA	X3-A17
I2C7_SCL	X3-A16
I2Cx_SDA	X2-A52
I2Cx_SCL	X2-A53

The following table shows the default I²C device addresses on the MBa95xxCA and the TQMa95xxLA.
For some devices the address can be changed by assembly options. The options are described in detail in the given chapter.

Table 9: I²C devices, address mapping on TQMa95xxLA and MBa95xxCA

Bus	Device	Component	Address	Note
I2C1	TQMa95xxLA	PMIC PF090x	0x08	
		PMIC PF5302	0x29	
		PMIC PF5301	0x2A	
		Temperature Sensor	0x1B	
		Temperature Sensor	0x53	
		Temperature Sensor	0x33	
	MBa95xxCA	Port Expander (Wake-up)	0x70	
		Starter Kit pin-header	NA	
I2C2	TQMa95xxLA	EEPROM (memory array)	0x54	
		EEPROM (identification page)	0x5C	
		RTC	0x51	
		TSE	0x48	
		Gyroscope	0x6B	
	MBa95xxCA	Audio Codec	0x18	
		USB-C PD-Controller	0x50	
		Temperature Sensor	0x1E	
		Temperature Sensor	0x56	
		Temperature Sensor	0x36	
		Port-Expander #1	0x74	
		Port-Expander #2	0x75	
		Port-Expander #3	0x76	
		PCIE Clock Generator	0x68	
		USB-Hub TUSB8041	0x44	Depending on the assignment of the strap pins for other options, addresses 0x45...0x47 may also be assigned
		USB-Hub USB2514	0x2C	
		Fan Controller	0x2F	
		10G ETH Retimer	0x1A	The address in the data sheet contains the R/W bit and is removed at this point
		10G ETH SFP+ Modul	0xA0 / 0xA2	Permitted addresses according to SFF-8431 specifications
		M.2 Key E Socket	NA	
		MIPI-DSI/CSI	NA	
		Starter Kit pin-header	NA	
I2C7	MBa95xxCA	Starter Kit pin-header	NA	

Note: I²C address conflicts	
	When changing the address due to assembly options or when connecting further I²C components, it must be ensured that no address conflicts occur. Otherwise malfunctions may occur. The addresses preassigned by the TQMa95xxLA must also be observed (depending on the TQMa95xxLA variant used).

3.4 GPIO port expander

Due to the limited number of GPIO pins available on the TQMa95xxLA, IO expanders are required to provide the necessary signals. A total of four I2C IO expanders are used on the MBa95xxCA. Only IO signals that need to be processed directly by the CPU (e.g. Interrupts, Timer IOs, PWM signals) are connected to the TQMa95xxLA. All other control signals are connected to the IO expanders.

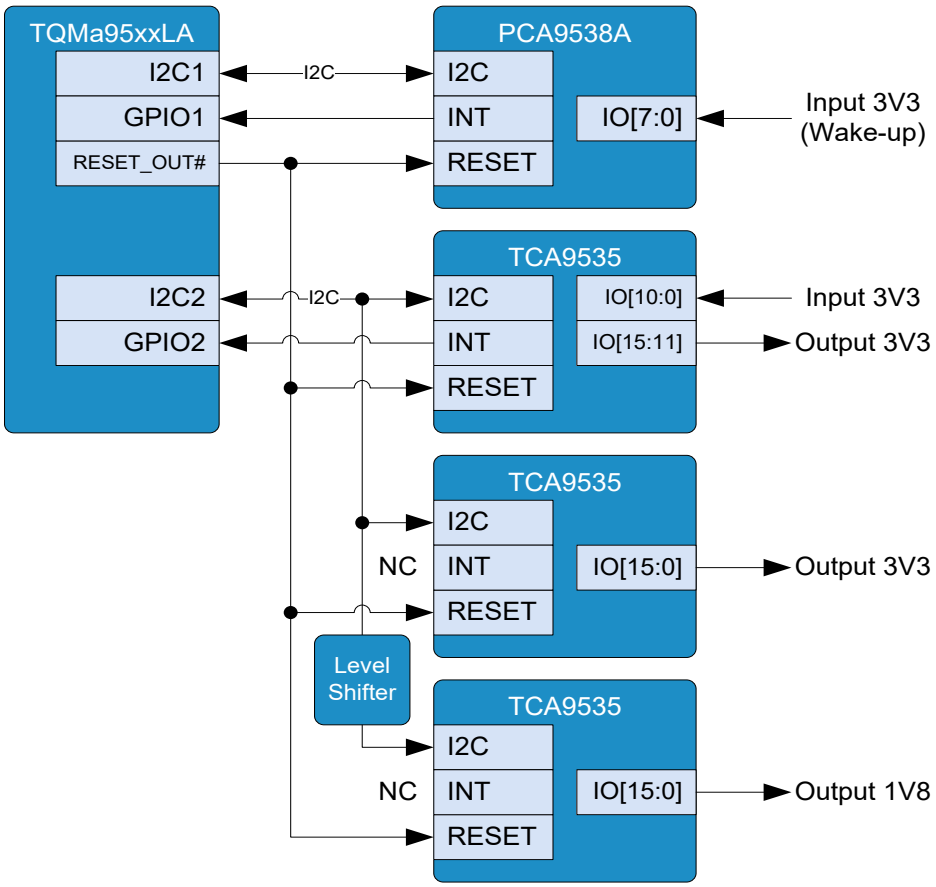


Figure 4: Block diagram GPIO expander

Signals that can be used to wake up the CPU are connected to an 8-port expander. This is connected to I2C1. The interrupt signal from the expander is connected to a CPU input of the GPIO1 group. This group, which also includes the I2C1 signals, is in the always-on domain, which remains active when the i.MX95 is in low-power mode. This allows the system to be reactivated with the wake-up signals.

Three further expanders on I2C2, each with 16 ports, are used for outputs and non-critical inputs. The input signals are connected to only one of the expanders and its interrupt signal is connected to a CPU input of the GPIO2 group. The other two expanders are used for outputs only. The interrupt pin of these two expanders is not connected to the CPU.

One of the output expanders is supplied with V_1V8 and is used for 1.8V output signals. The other three expanders are used for 3.3V signals and are therefore supplied with V_3V3. However, level converters are required for some signals.

The IO expanders used have a reset input connected to RESET_OUT#. This resets all signals when the CPU is reset (High-Z).

Table 10: Port expander functions

Expander	I²C device address	Port	Signal	Dir.	Level
1	0x70	IO_0	BUTTON_A#	I	3.3 V
		IO_1	TEMP_EVENT_MOD#		
		IO_2	GYRO_INT1_MOD		
		IO_3	M2_KEYE_SDIO_WAKE#		
		IO_4	M2_KEYE_UART_WAKE#		
		IO_5	M2_KEYE_PEWAKE#		
		IO_6	M2_KEYB_PEWAKE#		
		IO_7	M2_KEYB_WOWWAN#		
2	0x74	P00	BUTTON_B#	I	3.3 V
		P01	CAM0_SYNC_3V3	I	
		P02	CAM1_SYNC_3V3	I	
		P03	SFP_MOD_ABS	I	
		P04	DIG_IN1	I	
		P05	DIG_IN2	I	
		P06	DIG_IN3	I	
		P07	DIG_IN4	I	
		P10	DIG_OUT_1_2_STATE	I	
		P11	DIG_OUT_3_4_STATE	I	
		P12	DIG_OUT_1_EN	O	
		P13	DIG_OUT_2_EN	O	
		P14	DIG_OUT_3_EN	O	
		P15	DIG_OUT_4_EN	O	
		P16	AUDIO_RST#	O	
		P17	12V_EN	O	
3	0x75	P00	ETH10G_REFCLK_EN	O	3.3 V
		P01	ETH10G_REFCLK_RST#		
		P02	SFP_TX_DIS		
		P03	USB3_RESET#		
		P04	USB2_RESET#		
		P05	LCD_RESET#		
		P06	LCD_BLT_EN		
		P07	LCD_PWR_EN		
		P10	M2_KEYE_PERST#		
		P11	M2_KEYE_W_DISABLE1#		
		P12	M2_KEYE_W_DISABLE2#		
		P13	M2_KEYB_PERST#		
		P14	M2_KEYB_W_DISABLE1#		
		P15	USER_LED1		
		P16	USER_LED2		
		P17	3V3A_10G_EN		
4	0x76	P00	ENET1_RESET#	O	1.8 V
		P01	ENET2_RESET#		
		P02	M2_KEYE_SDIO_RST#		
		P03	M2_KEYE_DEV_WLAN_WAKE#		
		P04	M2_KEYE_DEV_BT_WAKE#		
		P05	M2_KEYB_W_DISABLE2#		
		P06	M2_KEYB_RST#		
		P07	M2_KEYB_FULL_CARD_PWR_OFF#		
		P10	M2_KEYB_DPR		
		P11	CAM0_PWR#		
		P12	CAM1_PWR#		
		P13	CAM0_RST#		
		P14	CAM1_RST#		
		P15	CAM0_TRIGGER		
		P16	CAM1_TRIGGER		
		P17	FAN_PWR_EN		

3.5 Temperature sensor and EEPROM

A temperature sensor SE97BTP is populated on the MBa95xxCA to monitor the temperature. The same type of sensor is also used on the TQMa95xxLA. The sensor of MBa95xxCA is read out via I2C2, the sensor of TQMa95xxLA is read out via I2C1, see Table 8.

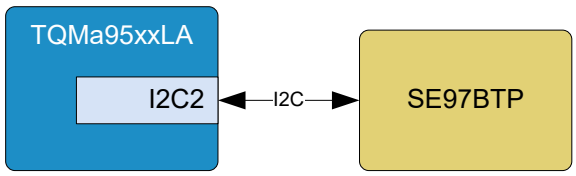


Figure 5: Block diagram temperature sensor

The sensor address on the MBa95xxCA can be changed by reassembling resistors (default `0b100`). When changing the address, care must be taken to avoid address conflicts with existing I²C devices, see Table 8. The assembly options are documented in the MBa95xxCA schematics.

The SE97BTP has an additional EEPROM. Further specifications of the SE97BTP can be found in the data sheet.

The alarm output EVENT# of the SE97BTP is available on the pin header X5 as TEMP_EVENT_MB#.

3.6 RTC backup

The TQMa95xxLA has an optional RTC. It is supplied via pin V_BAT.
On the MBa95xxCA there are two possibilities to supply the V_BAT input [1]:

- CR2032-Battery holder (X34)
- 2-pin header (X32) for alternative connection of an external voltage or batteries

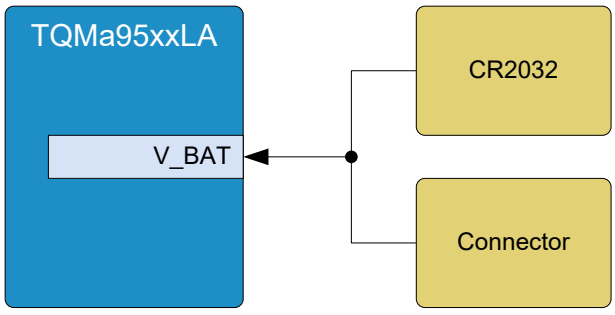


Figure 6: Block diagram RTC backup

Table 11: Pinout RTC backup (X34)

Pin	Signal	Level	Remark
1	V_BAT	3 V	Supply voltage for RTC on TQMa95xxLA
2	GND	0 V	Ground

To meet regulatory requirements for protection against accidental battery charging, a 1 kΩ resistor and diode is connected in series between X32/X34 and the V_BAT input of the TQMa95xxLA.
The diode has a very low forward voltage (<0.1 V) in order not to unnecessarily reduce the battery runtime and a very low reverse current to keep residual charging currents as low as possible.

1: Only one of the two options may be used at a time!

If it is necessary to reduce the forward voltage to 0 V for test purposes, the protective diode can be removed according to Table 12 and a corresponding resistor can be fitted.

Table 12: Assembly option RTC-Backup

Reverse current protection	V73	R299	Remark
Active	BAS70	NP	Default
Not active	NP	0 Ω	Note: 1 kΩ in series is still present in this case

Attention: Loss of reverse current protection	
	The reverse current protection is lost when the protective diode is replaced with a resistor! This is especially critical for TQMa95xxLA with external RTC, since here the 3.3 V supply of the TQMa95xxLA in ON mode drives directly into the RTC backup battery!

3.7 USB hub

The USB interfaces are implemented by cascading two USB hubs. The 4-port USB 3.0 hub TUSB8041 provides the USB 3.0 interfaces for the two USB host sockets and the M.2 Key B interface. Downstream, the USB2514 4-port USB 2.0 hub provides the USB 2.0 interfaces for the M.2 Key E interface, the LVDS CMD connector and the starter kit pin header.

The USB 3.0 hub is connected to the USB1 port and the USB_SS signals of the CPU. The USB 2.0 signals of the CPU's USB1 port are also switched to the USB Type-C interface to enable booting from the Serial Downloader (refer to chapter 3.18).

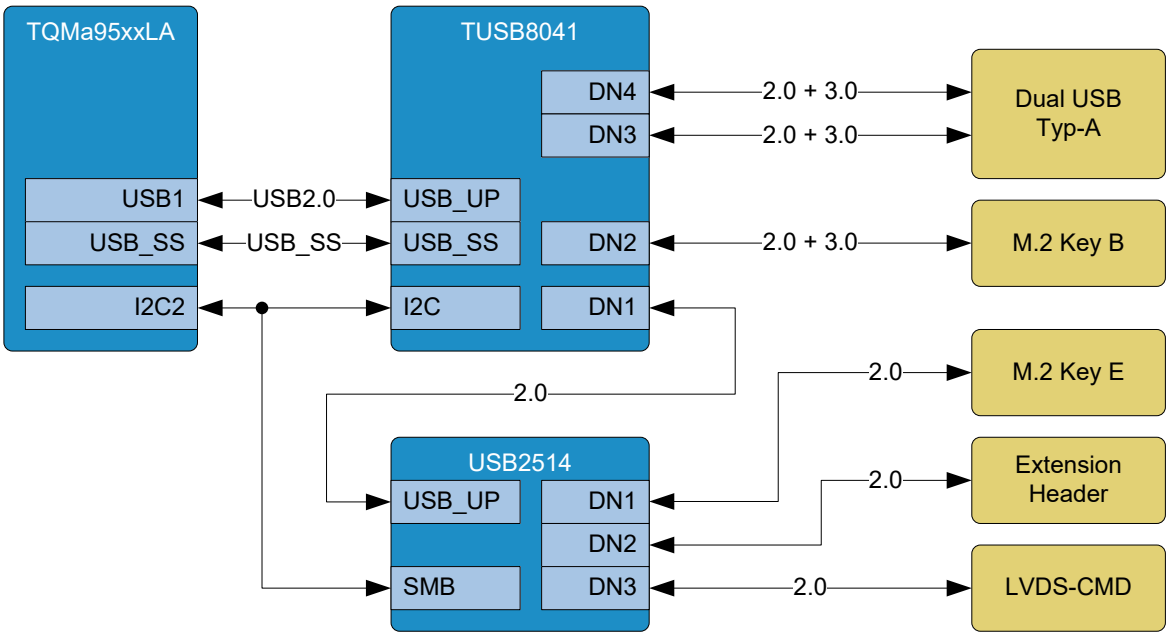


Figure 7: Block diagram USB hub

The USB1_OTG_PWR signal can be used by software to control the voltage at USB1_VBUS and at the detection pin of the USB hub TUSB8041. The signal at the detection pin of the USB2514 is controlled by the TUSB8041 due to the cascading.

As the USB 2.0 signals of the USB1 port are switched to the Type C interface when using the Serial Downloader, the voltage on USB1_VBUS must also be controlled by this interface in this case. For this purpose, the processed VBUS signal from USB Type C is linked by logic with the SEL_USB signal, which switches the USB signals in Serial Downloader mode, and used for control. The detection signal on USB2_VBUS is deactivated in this case.

3.8 CAN-FD

Both CAN interfaces of the MBa95xxCA are available at the two 3-pin connectors X13 and X14. Both interfaces are galvanically isolated with 1 kV. The CAN interfaces are not electrically isolated from each other.

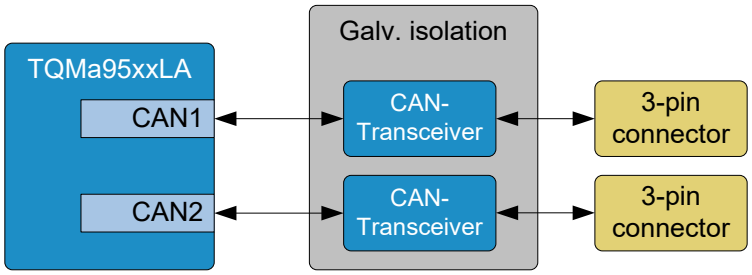


Figure 8: Block diagram CAN

The CAN signals can be terminated with DIP switches S6 (CAN1) and S7 (CAN2).

Table 13: CAN termination with S6/S7

Sx-1	Sx-2	Mode
OFF	OFF	No termination
OFF	ON	Not defined (irregular state)
ON	OFF	Not defined (irregular state)
ON	ON	Termination with 120 Ω

Table 14: Pinout CAN1 / 2 (X13, X14)

CAN	Pin	Signal	Dir.	Level	Remark
CAN0	1	CAN1_H	I/O	Spec. (1)	CAN High-Level I/O from CAN1 / galvanically isolated
	2	CAN1_L	I/O	Spec. (1)	CAN Low-Level I/O from CAN1 / galvanically isolated
	3	GND_CAN	P	0 V	Ground / galvanically isolated
CAN1	1	CAN2_H	I/O	Spec. (1)	CAN High-Level I/O from CAN2 / galvanically isolated
	2	CAN2_L	I/O	Spec. (1)	CAN Low-Level I/O from CAN2 / galvanically isolated
	3	GND_CAN	P	0 V	Ground / galvanically isolated

3.9 Debug USB / UART

For debug purposes, two UARTs of the i.MX95 CPU are made available at USB socket X26 by using an UART-USB-Bridge CP2105 from Silicon Labs. UART1 and UART2 are used for this purpose.

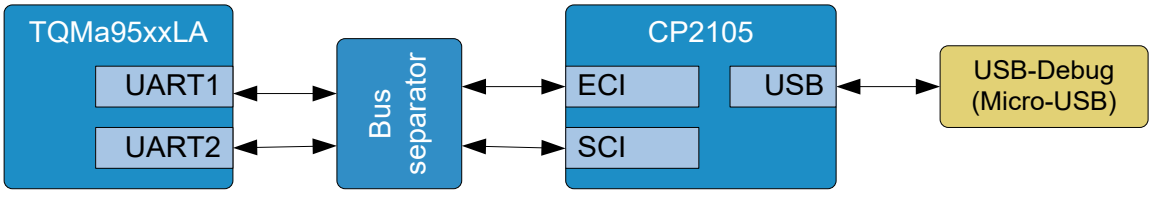


Figure 9: Block diagram USB debug

3.10 1Gb Ethernet

The i.MX95 processor has two independent RGMII interfaces. On the MBa95xxCA, both interfaces are used to provide two Gigabit Ethernet ports (X10/X11) with Time Sensitive Network (TSN) features.

The Ethernet ports are provided on two RJ45 sockets.

1: According to CAN standard.

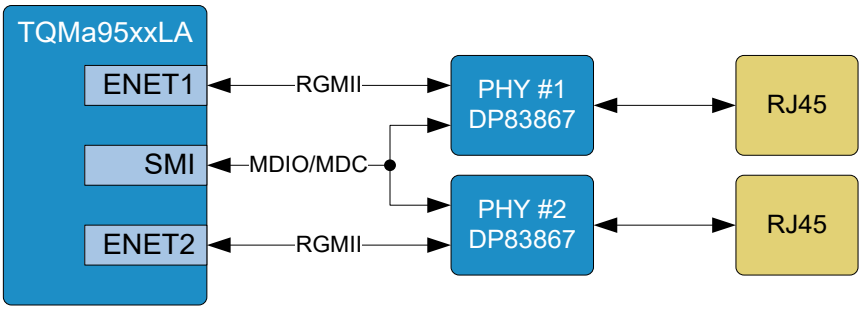


Figure 10: Block diagram Ethernet

The used PHY DP83867 is TSN compliant. However, the required TSN features are mainly on the MAC and application level. The DP83867 has configurable GPIO signals that can be used as SFD (Start of Frame) detection outputs for debugging purposes. For Ethernet1 interface, these signals are provided on solder pads (X31) on the MBa95xxCA.

3.11 10Gb Ethernet / SFP+

The 10Gb Ethernet interface is implemented as an SFP+ standard interface. This allows the user to choose between different SFP+ modules (e.g. modules for fiber optic cable or for copper cable). The 10Gb interface of the CPU is TSN capable.

The TX and RX data signals of the CPU's XGMII are routed to the SFP+ connector via a retimer. The retimer compensates for insertion loss and performs signal conditioning.

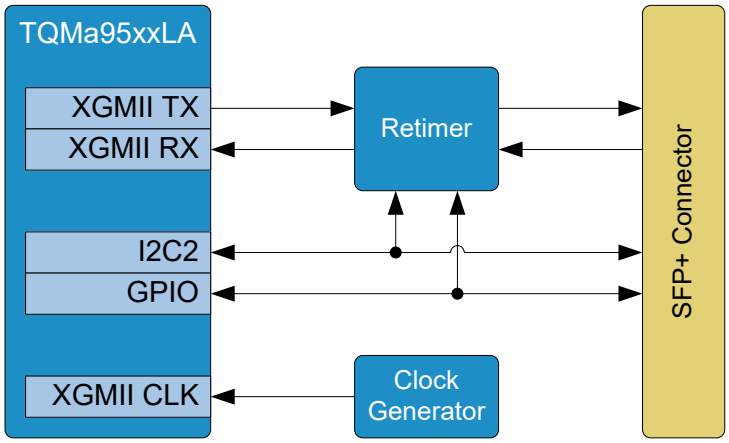


Figure 11: Block diagram 10G Ethernet

The control signals of the retimer and the SFP+ connector (X12/X35) are connected to the TQMa95xxLA via GPIO or I2C port expander.

The SFP+ management interface conforms to the I2C standard and is therefore connected via I2C. The specification gives the addresses 0xA0 and 0xA2 as I2C device addresses.

Table 15: I2C device addresses for SFP+ module

Address	(MSB)						Address Select	R/W Select (LSB)
A0h	1	0	1	0	0	0	0	x
A2h	1	0	1	0	0	0	1	x

3.12 LVDS

The i.MX 95 processor has two LVDS interfaces with four lanes each. These are provided on the MBa95xxCA as dual LVDS on one connector (X19).

The MBa95xxCA also has an additional CMD connector (X20), similar to other existing mainboards, which provides power, USB, and display/backlight control signals.

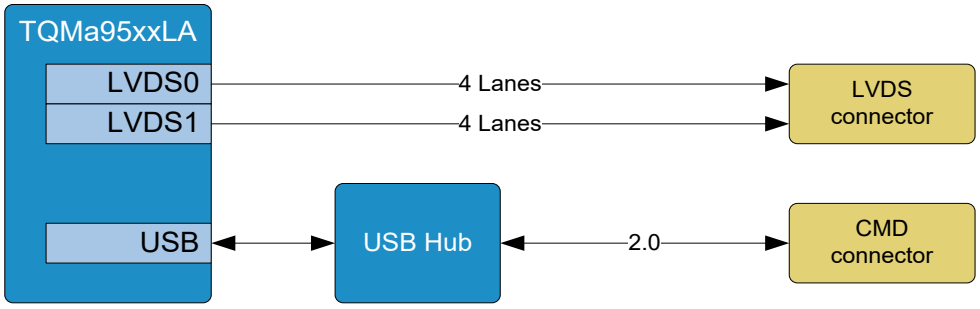


Figure 12: Block diagram LVDS

Table 16: Pinout LVDS Data (X19)

Pin	Signal	Dir.	Level	Remark
1	LVDS0_DATA0–	O	1.8 V	LVDS0 interface (Lane 0)
2	LVDS0_DATA0+	O	1.8 V	
3	LVDS0_DATA1–	O	1.8 V	LVDS0 interface (Lane 1)
4	LVDS0_DATA1+	O	1.8 V	
5	LVDS0_DATA2–	O	1.8 V	LVDS0 interface (Lane 2)
6	LVDS0_DATA2+	O	1.8 V	
7	GND	P	0 V	Ground
8	LVDS0_CLOCK–	O	1.8 V	LVDS0 interface (Clock)
9	LVDS0_CLOCK+	O	1.8 V	
10	LVDS0_DATA3–	O	1.8 V	LVDS0 interface (Lane 3)
11	LVDS0_DATA3+	O	1.8 V	
12	LVDS1_DATA0–	O	1.8 V	LVDS1 interface (Lane 0)
13	LVDS1_DATA0+	O	1.8 V	
14	GND	P	0 V	Ground
15	LVDS1_DATA1–	O	1.8 V	LVDS1 interface (Lane 1)
16	LVDS1_DATA1+	O	1.8 V	
17	GND	P	0 V	Ground
18	LVDS1_DATA2–	O	1.8 V	LVDS1 interface (Lane 2)
19	LVDS1_DATA2+	O	1.8 V	
20	LVDS1_CLOCK–	O	1.8 V	LVDS1 interface (Clock)
21	LVDS1_CLOCK+	O	1.8 V	
22	LVDS1_DATA3–	O	1.8 V	LVDS1 interface (Lane 3)
23	LVDS1_DATA3+	O	1.8 V	
24	GND	P	0 V	Ground
25	V_5V_LVDS	P	5 V	5 V supply voltage (1 A max. output)
26	V_5V_LVDS	P	5 V	
27	V_5V_LVDS	P	5 V	
28	V_3V3_LVDS	P	3.3 V	3.3 V supply voltage (1 A max. output)
29	V_3V3_LVDS	P	3.3 V	
30	V_3V3_LVDS	P	3.3 V	
M1, M2	GND	P	0 V	Ground

Table 17: Pinout LVDS CMD (X20)

Pin	Signal	Dir.	Level	Remark
1	V_12V	P	12 V	12 V supply voltage (2.5 A max.)
2	V_12V	P	12 V	
3	V_12V	P	12 V	
4	GND	P	0 V	Ground
5	GND	P	0 V	
6	GND	P	0 V	
7	V_5V_MB	P	5 V	5 V supply voltage (1 A max.)
8	V_5V_MB	P	5 V	
9	GND	P	0 V	Ground
10	GND	P	0 V	
11	V_VBUS_H7	P	5 V	VBUS USB Host 7 (0.5 A max.)
12	GND	P	0 V	Ground
13	USBH7_D–	I/O	3.3 V	Data USB Host 7
14	USBH7_D+	I/O	3.3 V	
15	GND	P	0 V	Ground
16	LCD_RESET#	O_{PD}	3.3 V	Reset
17	LCD_BLT_EN	O_{PD}	3.3 V	Backlight-Enable
18	LCD_PWR_EN	O_{PD}	3.3 V	Power-Enable
19	LCD_PWM	O	3.3 V	PWM Contrast-/ Brightness
20	GND	P	0 V	Ground
M1, M2	GND	P	0 V	Ground

3.13 Audio

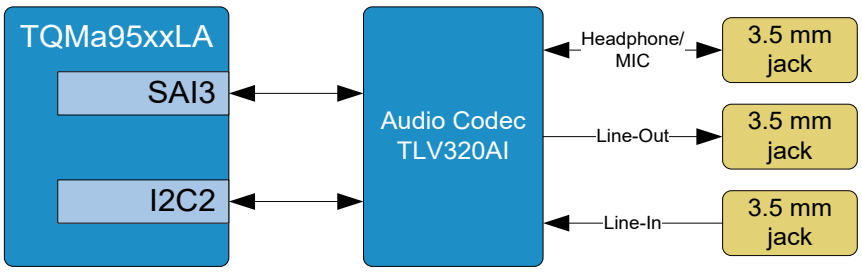


Figure 13: Block diagram Audio

The TLV320AI audio codec connects to the CPU's SAI interface. Three jacks (Lumberg 1503 31) are provided for line in, line out and headphone/MIC. The headphone output is connected to a combined headphone/MIC jack. This socket is wired according to the CTIA standard.

Table 18: Pin out audio jacks

Pin	Socket X22 (phone/mic)	Socket X23 (line in)	Socket X24 (line out)
1	MIC_IN	AGND_AUD	AGND_AUD
2	AGND_AUD	AGND_AUD	AGND_AUD
3	HEADPHONE_R	LINE_IN_R	LINE_OUT_R
4A, 4B	HEADPHONE_L	LINE_IN_L	LINE_OUT_L

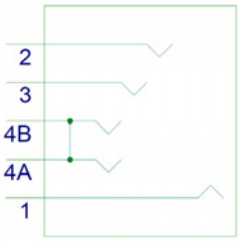


Figure 14: Pinning 3.5 mm jack

3.14 MIPI DSI/CSI

The i.MX 95 processor has two MIPI interfaces, each with four lanes: a MIPI-CSI interface and a shared interface for MIPI-DSI/CSI. Both interfaces are available on the MBa95xxCA on the common connector X21 (Tyco Electronics 5177986-2).

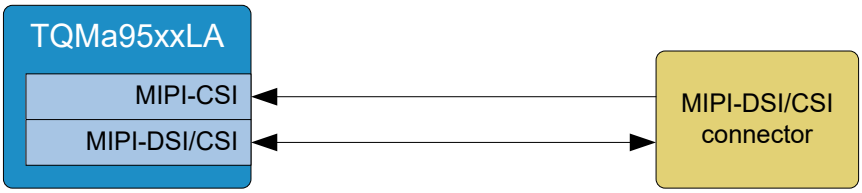


Figure 15: Block diagram MIPI CSI

Table 19: Pinout MIPI-CSI (X21)

Signal	Pin	Pin	Signal
GND	1	2	GND
CAM0_PWR#	3	4	CAM1_PWR#
CAM0_RST#	5	6	CAM1_RST#
CAM0_TRIGGER	7	8	CAM1_TRIGGER
CAM0_SYNC	9	10	CAM1_SYNC
(NC)	11	12	(NC)
GND	13	14	GND
MIPI_CSI1_DATA3-	15	16	MIPI_DSICSI1_DATA3-
MIPI_CSI1_DATA3+	17	18	MIPI_DSICSI1_DATA3+
GND	19	20	GND
MIPI_CSI1_DATA2-	21	22	MIPI_DSICSI1_DATA2-
MIPI_CSI1_DATA2+	23	24	MIPI_DSICSI1_DATA2+
GND	25	26	GND
MIPI_CSI1_DATA1-	27	28	MIPI_DSICSI1_DATA1-
MIPI_CSI1_DATA1+	29	30	MIPI_DSICSI1_DATA1+
GND	31	32	GND
MIPI_CSI1_DATA0-	33	34	MIPI_DSICSI1_DATA0-
MIPI_CSI1_DATA0+	35	36	MIPI_DSICSI1_DATA0+
GND	37	38	GND
MIPI_CSI1_CLOCK-	39	40	MIPI_DSICSI1_CLOCK-
MIPI_CSI1_CLOCK+	41	42	MIPI_DSICSI1_CLOCK+
GND	43	44	GND
I2C2_1V8_SDA	45	46	I2C2_1V8_SDA
I2C5_1V8_SCL	47	48	I2C5_1V8_SCL
GND	49	50	GND
CAM0_MCLK	51	52	CAM1_MCLK
GND	53	54	GND
V_1V8 (optional)	55	56	V_V5_MB
V_3V3 (optional)	57	58	V_V5_MB
V_3V3 (optional)	59	60	V_V5_MB

3.15 M.2 interfaces

The MBa95xxCA provides one M.2 Key E slot with PCIe, USB 2.0 and SDIO for WiFi and one M.2 Key B slot with PCIe, USB 3.0/2.0 and SIM card for cellular. WiFi modules with Key A+E can also be used in the M.2 Key E slot.

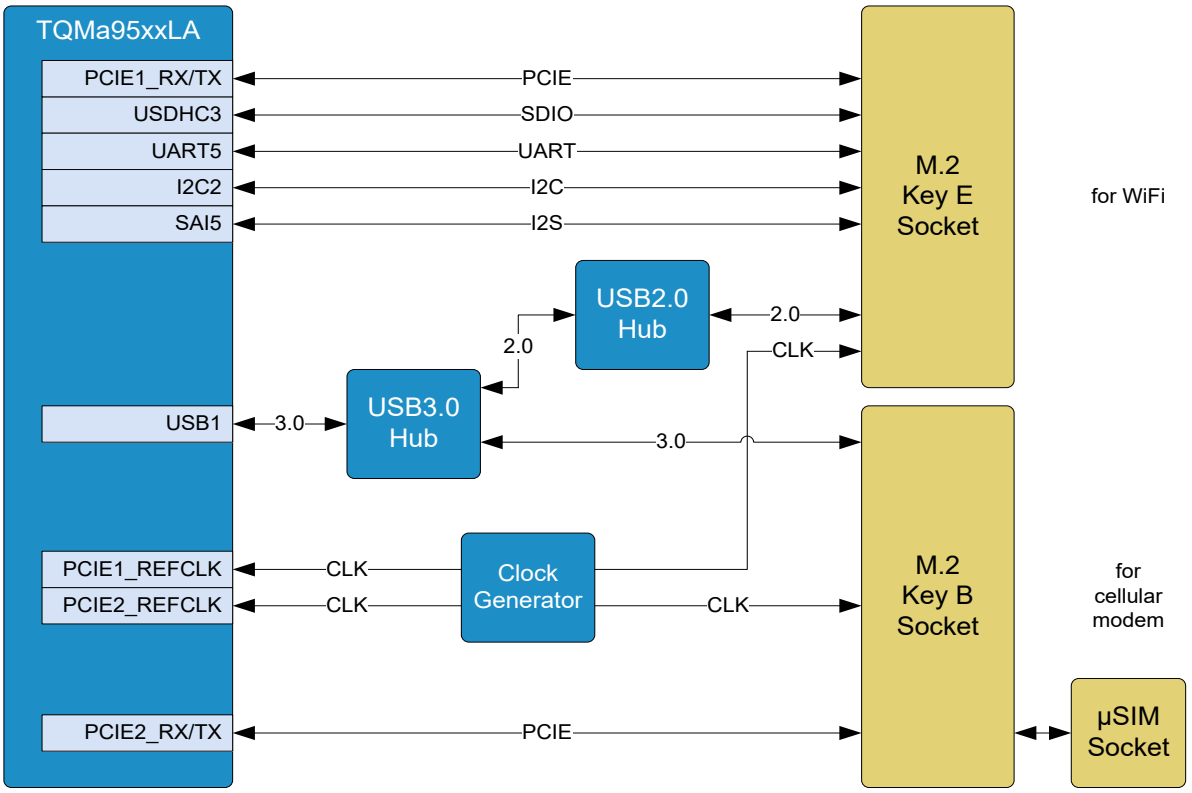


Figure 16: Block diagram M.2

3.16 SIM card

A Micro-SIM card holder (X18) is available on the MBa95xxCA for the use of a SIM card, which is directly connected to the M.2 Key B slot.

3.17 USB Host

The required USB interfaces for the host ports are provided by the USB hub (see chapter 3.7). VBUS with max. 900 mA each is provided at the double-decker USB type A host connectors. An AP2171 power switch is used for each. The current limit is internally set to typ. 1.5 A, the recommended maximum continuous current is 1 A.

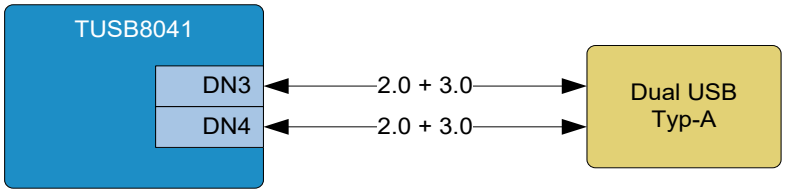


Figure 17: Block diagram USB Host

3.18 USB Type-C

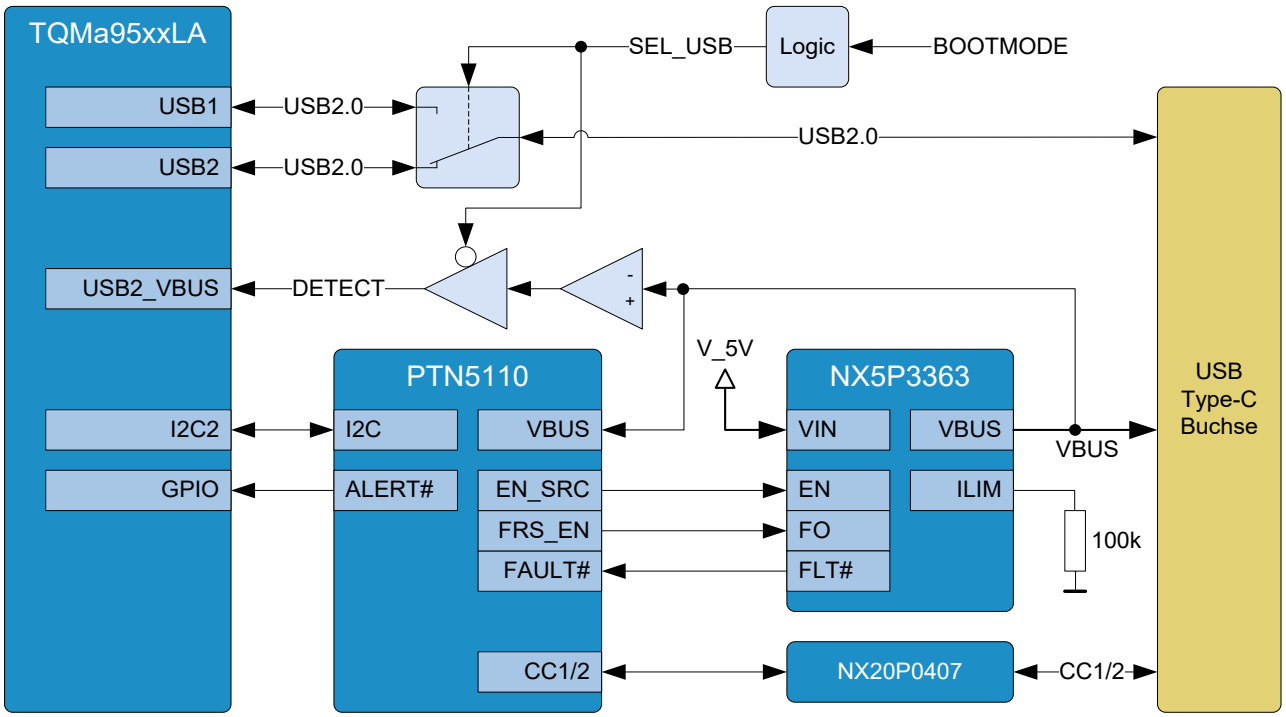


Figure 18: Block diagram USB Type-C

The USB Type-C interface is connected to the USB2 interface of the CPU by default. This means that the connector X9 is used for USB 2.0 signals only. However, as this interface should also be available for the serial downloader, the USB 2.0 signals of the USB1 interface of the CPU are routed to the socket via an analog switch in serial downloader mode. USB2 is not supported by the serial downloader. To switch over, the BOOTMODE signals are logically linked and sent to the analog switch as a control signal.

Table 20: Logic USB Type-C port

BOOT_MODE[3:0]	USB Port	Boot Device
x001	USB1	Serial Downloader
xxx0	USB2	Other Boot Devices
x011		
x101		
x111		

3.19 Micro-SD card

The micro SD card connector (X7) is directly connected to the uSDHC2 interface of the TQMa95xxLA. A 4-bit wide data interface is used. The uSDHC controller in the i.MX95 supports UHS-I mode.

The switching of the IO voltage is performed by the module-internal signal SD2_VSELECT. No measures are necessary on the mainboard for this. The SD card is supplied with V_3V3_SD, which is provided by the TQMa95xxLA.

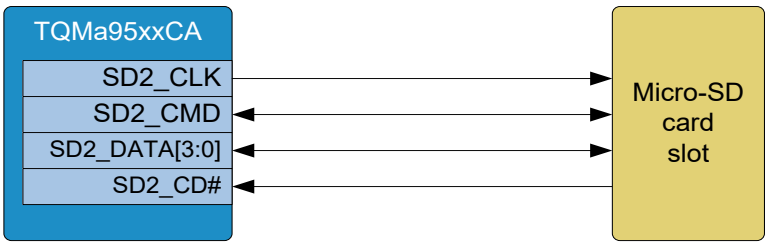


Figure 19: Block diagram Micro-SD card

3.20 RS485

On the MBa95xxCA, a RS485 interface (halfduplex) is realized. This interface is not galvanically isolated. It is connected to the UART8 interface of the TQMa95xxLA. The RTS signal of the UART interface (possibly used as GPIO) is used for automatic direction switching.

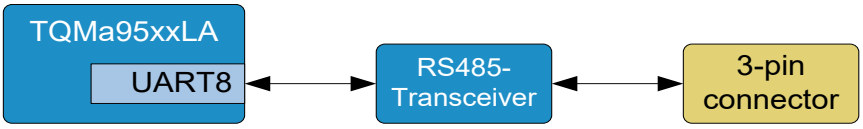


Figure 20: Block diagram RS485

The bus termination for RS485 is done via DIP switch S8. By default the termination (120 Ω) components are equipped to use it for RS485 bus. There is a assembly option to use a Profibus compliant termination. The assembly option is documented in the MBa95xxCA schematic.

The RS485 Bus is provided at a 3-pin connector.

Table 21: Pinout RS485 (X15)

Pin	Signal
1	RS485_A
2	RS485_B
3	GND

Table 22: Termination switch S8

S8-1	S8-2	Modus
OFF	OFF	No bus termination
OFF	ON	Not defined (irregular state)
ON	OFF	Not defined (irregular state)
ON	ON	Bus terminated

3.21 MBa95xxCA Extension Headers (X4, X5, X6)

The MBa95xxCA provides three 100 mil headers. In addition to the signals, 1.8V, 3.3V, 5V and 12V are available on the headers. The maximum current is divided among all pin headers as well as the connectors of LVDS, MIPI-DSI/CSI, and analog input. In total, no more than the specified maximum current may be drawn at the following interfaces:

Table 23: Power consumption headers

Rail	I_{max}	Remark
V_12V	2.5 A	Sum of currents at X4, X5, X20, X30
V_5V_MB	2 A	Sum of currents at X4, X5, X19, X20, X21, (X30)
V_3V3	2 A	Sum of currents at X4, X5, X19, X21
V_1V8	250 mA	Sum of currents at X4, X5, X6, X21

Note: Observe power consumption with regard to the overall system	
	The supply voltages (1.8 V, 12 V, etc.) provided at the MBa95xxCA headers are not individually fused. Technically, an overload of the fuse at the 24 V supply input is therefore possible, see also chapter 3.26. Please note the resulting total current consumption of the MBa95xxCA, which must be less than 5 A!

Table 24: Pinout extension header X4

Level	Signal	Pin		Signal	Level
12 V	V_12V	1	2	V_3V3_MB	5 V
5 V	V_5V_MB	3	4	V_1V8	1.8 V
0 V	GND	5	6	GND	0 V
1.8 V	XSPI_SS0#	7	8	I2C2_SCL	3.3 V
1.8 V	XSPI_DATA0	9	10	I2C2_SDA	3.3 V
1.8 V	XSPI_DATA1	11	12	I2C1_ SCL	3.3 V
1.8 V	XSPI_DATA2	13	14	I2C1_ SDA	3.3 V
1.8 V	XSPI_DATA3	15	16	I2CX_ SCL	3.3 V
1.8 V	XSPI_SCK	17	18	I2CX_ SDA	3.3 V
0 V	GND	19	20	I2C7_ SCL	3.3 V
1.8 V	SAI5_TXD0	21	22	I2C7_ SDA	3.3 V
1.8 V	SAI5_RXD0	23	24	CAN4_TX	3.3 V
1.8 V	SAI5_TX_SYNC	25	26	CAN4_RX	3.3 V
1.8 V	SAI5_RX_SYNC	27	28	GND	0 V
1.8 V	SAI5_TX_BCLK	29	30	SPI4_PCS0#	3.3 V
1.8 V	SAI5_RX_BCLK	31	32	SPI4_PCS1#	3.3 V
0 V	GND	33	34	SPI4_SIN	3.3 V
3.3 V	USB_H6_D+	35	36	SPI4_SOUT	3.3 V
3.3 V	USB_H6_D-	37	38	GND	0 V
5 V	V_VBUS_H6	39	40	SPI4_SCLK	3.3 V

Table 25: Pinout extension header X5

Level	Signal	Pin		Signal	Level
12 V	V_12V	1	2	V_3V3	3.3 V
5 V	V_5V_MB	3	4	V_1V8	1.8 V
0 V	GND	5	6	GND	0 V
3.3 V	TEMP_EVENT_MB#	7	8	RESET_OUT#	3.3 V
3.3 V	FAN_ALERT#	9	10	RESET_IN#	1.8 V
3.3 V	M33_NMI	11	12	IMX_ONOFF	1.8 V
3.3 V	WDOG_ANY	13	14	PMIC_ON_REQ	1.8 V
3.3 V	PGOOD	15	16	SD2_RESET#	V_SD
1.8 V	TAMPER1	17	18	GND	3.3 V
1.8 V	TAMPER0	19	20	EARC_P_UTIL	1.8 V
0 V	GND	21	22	EARC_N_HPD	1.8 V
3.3 V	UART7_TX	23	24	EARC_AUX	1.8 V
3.3 V	UART7_RX	25	26	GND	0 V
3.3 V	UART7_CTS#	27	28	TSE_ISO_7816_CLK	3.3 V
3.3V	UART7_RTS#	29	30	TSE_ISO_7816_IO1	3.3 V
-	RFU	31	32	TSE_ISO_7816_IO2	3.3 V
3.3 V	HEADER_PWM	33	34	TSE_ISO_7816_RST#	3.3 V
0 V	GND	35	36	GND	0 V
1.8 V	CCM_CLK03	37	38	CLK_IN1	1.8 V
1.8 V	CCM_CLK04	39	40	CLK_IN2	1.8 V

Table 26: Pinout extension header X6

Level	Signal	Pin		Signal	Level
1.8 V	V_1V8_A	1	2	V_1V8_A	1.8 V
1.8 V	ADC_IN2	3	4	ADC_IN5	1.8 V
1.8 V	ADC_IN3	5	6	ADC_IN6	1.8 V
1.8 V	ADC_IN4	7	8	ADC_IN7	1.8 V
0 V	GND	9	10	GND	0 V

3.22 IO Header X25

The X25 pin header provides an IO extension with four digital inputs, four digital outputs, and two analog inputs designed for higher voltages (up to 32 V).

Table 27: Pinout IO header X25

Level	Signal	Pin		Signal	Level
V = 16…32 V I = 2 A (max.)	V_24V_OUT	B1	A1	GND	0 V
		B2	A2		
V = 16…32 V I = 2 A (max.)	V_HSS_IN	B3	A3		
		B4	A4		
0 V	GND	B5	A5		
V_HSS_IN (max. 500 mA per channel)	DIG_OUT_1	B6	A6		
	DIG_OUT_2	B7	A7		
	DIG_OUT_3	B8	A8		
	DIG_OUT_4	B9	A9		
max. 32 V	DIG_IN_1	B10	A10		
	DIG_IN_2	B11	A11		
	DIG_IN_3	B12	A12		
	DIG_IN_4	B13	A13		
0…32 V	ANA_IN1	B14	A14		
	ANA_IN2	B15	A15		

Table 28: Threshold digital inputs

Threshold	min.	typ.	max.
Positive	-	11.25 V	13.86 V
Negative	3.35 V	6.19 V	-

3.23 JTAG

The JTAG interface is routed to a 10-pin header (X27). All signal lines use 1.8 V as reference voltage. The JTAG interface is not ESD protected.

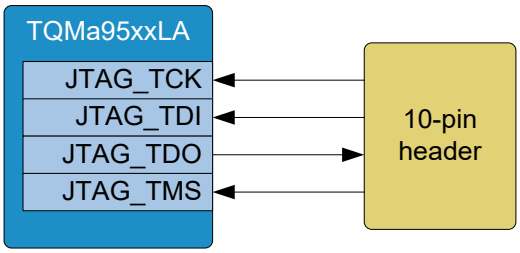


Figure 21: Block diagram JTAG

Table 29: Pinout JTAG (X20)

Remark	Level	Dir.	Signal	Pin	Pin	Signal	Dir.	Level	Remark
Test Mode Select	1.8 V	I_{PU}	JTAG_TMS	2	1	V_1V8	P	1.8 V	1.8 V
Test Clock	1.8 V	I_{PD}	JTAG_TCK	4	3	GND	P	0 V	Ground
Test Data Out	1.8 V	O	JTAG_TDO	6	5	GND	P	0 V	Ground
Test Data In	1.8 V	I_{PU}	JTAG_TDI	8	7	(NC)	–	–	Not used
Not used	-	-	(NC)	10	9	GND	P	0 V	Pulled to ground

3.24 Fan

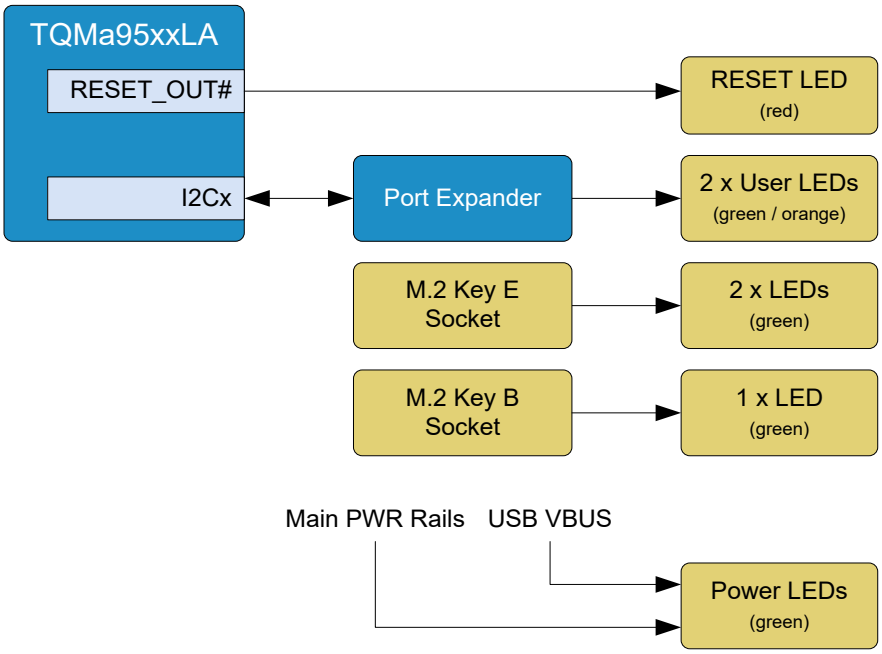
If active cooling of the TQ module is required, a fan connector is provided. The fan is controlled by a fan controller. The fan connector has both a PWM and a tacho signal. The fan is connected to a 4-pin Molex connector and is supplied with 12 V as standard. Optionally, 5 V can be used via placement option. The fan is mounted on the optional heat sink of the TQMa95xxLA. Mounting holes are provided on the mainboard.

Table 30: Pinout fan header (X30)

Signal	Pin
GND	1
V_FAN	2
RPM	3
PWM	4

3.25 Status LEDs

Several LEDs are provided on the MBa95xxCA. In addition to an LED for RESET_OUT# and LEDs on the M.2 sockets, there are two user LEDs that can be controlled via IO expanders. Furthermore, one LED is provided on each of the main voltage rails and the VBUS voltages of all USB ports. These LEDs signal to the user that the voltages have reached the typical end value and facilitate development on the MBa95xxCA as well as troubleshooting.



3.26 User Buttons

Two short-stroke keys are provided for simple user input. The buttons are connected to the IO expander as the available GPIO pins of the TQMa95xxLA are very limited.

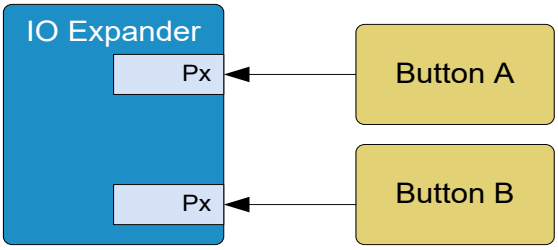


Figure 22: Block diagram user buttons

3.27 Power supply

The MBa95xxCA must be supplied with 24 V DC (typ.) via one of the two connections X28 and X29, which can be used alternatively.

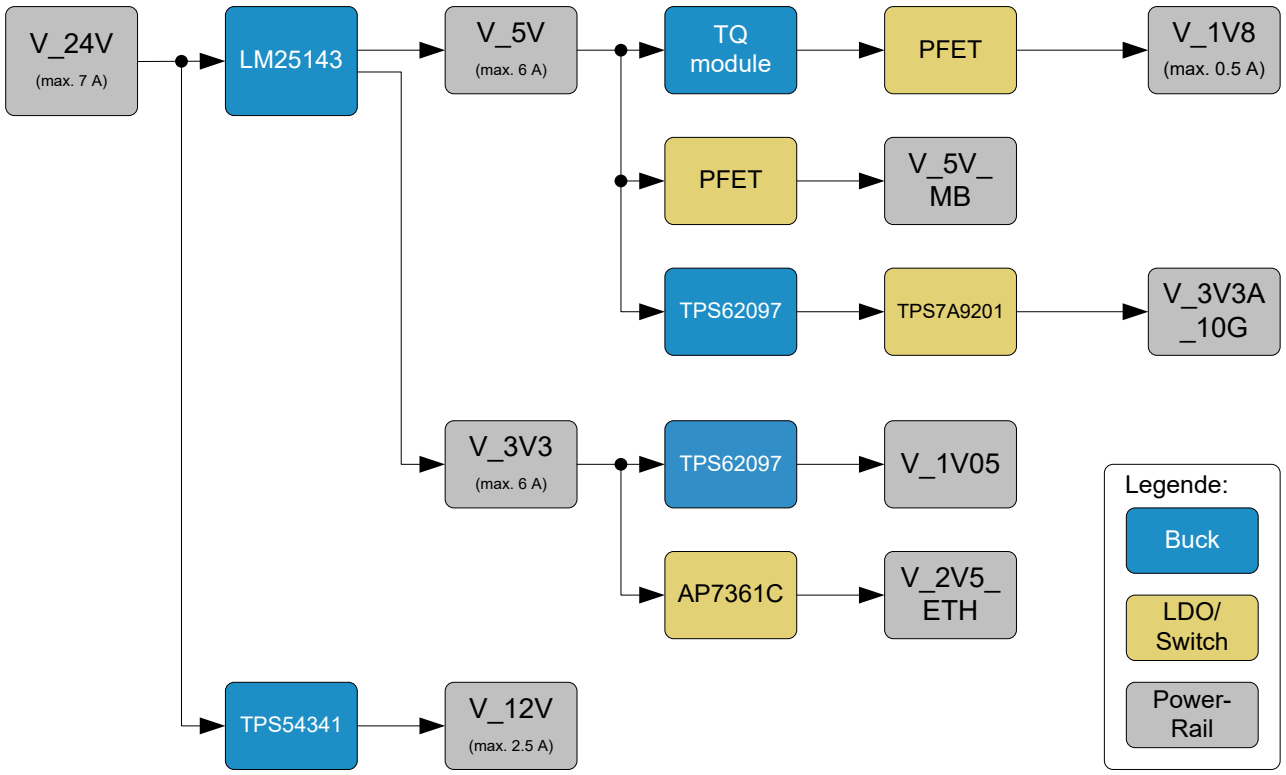


Figure 23: Block diagram MBa95xxCA power supply

Figure 24 shows all voltages (rails) on the MBa95xxCA, which are divided into two main paths consisting of a LM25143 and a TPS54341. These supply the largest loads (TQMa95xxLA, USB supply, 12 V display supply).

The design also allows power sequencing of all voltage levels used. With the exception of V_5V, all voltages are switched on after the TQMa95xxLA boots. A 1.8 V supply is already provided by the TQMa95xxLA and delivers up to 500 mA.

3.27.1 Input protection

The following protective circuits are provided for the input voltage V_24V of the MBa95xxCA:

- Fuse 7 A, slow blow
- Overvoltage protection
- PI Filter (CLC element)
- Reverse polarity protection
- Voltage stabilization

Attention: Voltages at headers	
	The internal voltages (1.8 V, 12 V, etc.) provided at the MBa95xxCA headers are not separately fused. Technically an overload of the fuse is therefore possible. The resulting total current consumption of the MBa95xxCA should be kept below 7 A in total.

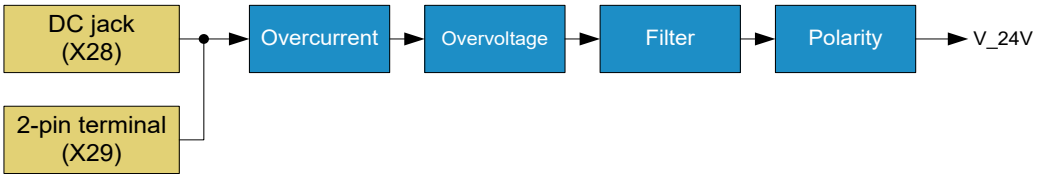


Figure 24: Block diagram Power-In

Table 31: Supply voltage V_24V_IN at Power-In (X28, X29)

Parameter	Min.	Typ.	Max.	Remark
Input voltage	16 V	24 V	32 V	–
Power consumption	–	TBD (1)	TBD (2)	–
Rated current of the fuse	–	7 A	–	–
Voltage limitation in case of overvoltage	TBD	–	TBD	Note: The MBa95xxCA may be damaged in case of permanent overvoltage!

Table 32: Pinout power-in (X28, X29)

Pin	Pin	Signal	Type	Level	Remark
X28	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground
	3	(NC)	–	–	Not connected
X29	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground

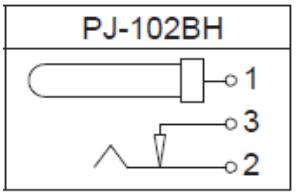


Figure 25: Pinout DC socket 2.5 mm/6.5 mm

1: Typical scenario is not defined.
2: Theoretical full load. All supply voltages are loaded with maximum current, e.g. by connecting additional load to the pin headers, and all system components have maximum power consumption.

3.27.2 Power sequencing

The following figure shows the power-on sequences of the different voltage levels of the main board, without taking into account the rise times of the voltages:

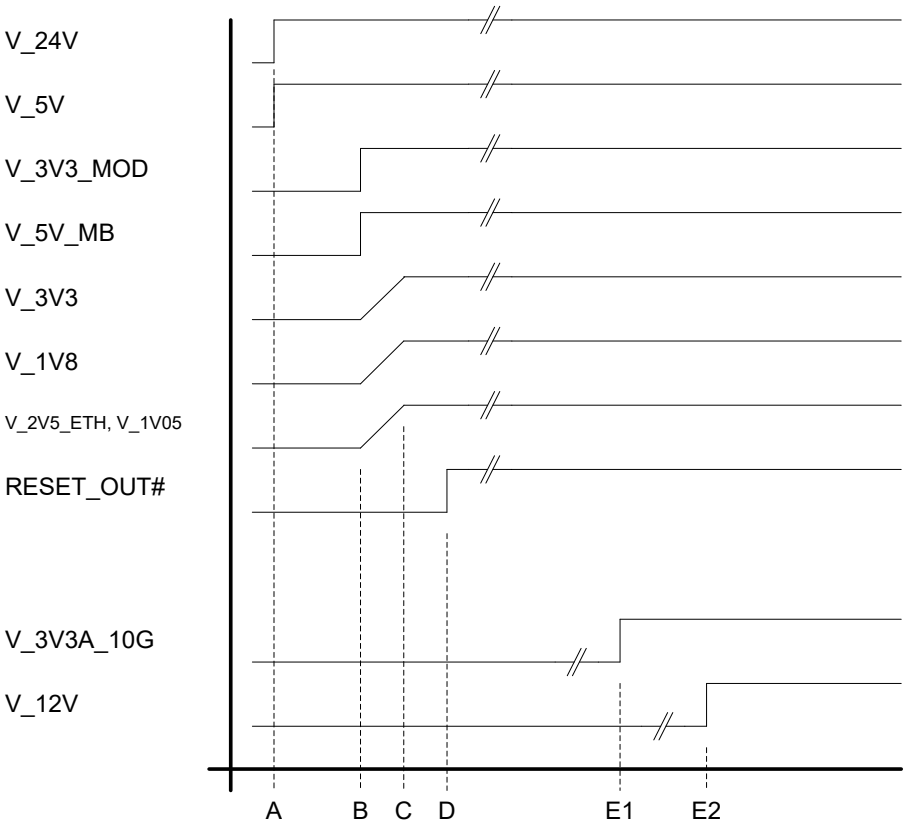


Figure 26: Power sequencing MBa95xxCA

The following table shows the sequence steps from Figure 26:

Table 33: Power sequencing

Sequence	Time	Description
A	–	Start point: Power-up MBa95xxCA supplies.
B	8.4 ms (t_B)	Release MBa95xxCA supplies by V_3V3_MOD as last part of the internal power sequence of the TQMa95xxLA.
C	t_B + 1 ms	MBa95xxCA supply stable (Softstart Time V_3V3)
D	t_B + 1.2 ms	Release RESET_OUT# after completion of TQMa95xxLA power sequencing.
E1, E2	Software dependent	Switching on of additional supply by software driver with signals 3V3A_10G_EN and 12V_EN.

V_3V3_MOD controls the second regulator of the LM25119 (V_3V3) as well as the power FET for V_5V_MB by means of supervisor. Automatically V_2V5_ETH and V_1V05 are activated. V_1V8 is activated by V_2V5_ETH.

Determined by the internal power sequence of the TQMa95xxLA, RESET_OUT# is released 1.2 ms after the voltage level V_3V3_MOD (TQMa95xxLA internal V_3V3) is switched on. The power-up of the mainboard voltages is completed approx. 1 ms after V_3V3_MOD. Thus all necessary voltages on the TQMa95xxLA and the MBa95xxCA are stable when the system starts.

3.27.3 V_5V and V_3V3

3.3 V and 5 V are required to supply the TQMa95xxLA, some components on the mainboard and the USB voltage. The dual regulator LM25143 is used for this purpose, which generates the two voltages from the 16...32 V input voltage.
The voltage V_5V is automatically activated when the mainboard supply is switched on and supplies the TQMa95xxLA. V_3V3 is activated after completion of the module-internal power sequencing with the V_3V3_MOD provided by the module by means of supervisor (LM25119 pin EN2). The designs have the following specification:

Table 34: Specifications V_5V and V_3V3

Voltage	Parameter	Value	Remark
V_5V	V_{IN}	16…32 V	V_24V
	V_{OUT}	4.95…5.05 V	V_5V
	I_{OUT}	6 A	Load: 5.2 A (realistic use case)
V_3V3	V_{IN}	16…32 V	V_24V
	V_{OUT}	3.267…3.335 V	V_3V3
	I_{OUT}	6 A	Load: max. 5.2 A (realistic use case)

3.27.4 V_5V_MB

Besides the module, the mainboard needs a 5 V supply for some components. This voltage V_5V_MB is switched on after completion of the module-internal power sequencing.
Components whose power is not switched via separate enable signals are supplied from V_5V_MB. The power distribution switches for USB and the DCDC for V_3V3A_10G are powered directly from V_5V.

3.27.5 V_1V8

Because the power requirement by the components on the mainboard for 1.8 V is very low, the 1.8 V provided by the TQMa95xxLA is used for V_1V8. The module supplies up to 500 mA. A maximum of 250 mA of this remains for the starter kit header. As the 1.8 V are switched on by the module at an early stage in sequencing, they must be activated with a delay for the mainboard components. Otherwise, the power timing of the Ethernet PHYs will be violated. V_1V8_MOD is therefore switched on with a P-channel FET by V_2V5_ETH.

3.27.6 V_3V3A_10G

The 3.3 V supply voltage for the XGMII Retimer and the SFP+ module is generated by a step-down converter (V_3V6_10G) and a downstream LDO (V_3V3A_10G). The step-down converter can be enabled by software using a GPIO signal.
The design has the following specification:

Table 35: Specification V_3V6_10G / V_3V3_10G

Voltage	Parameter	Value	Remark
V_3V6_10G	V_{IN}	typ. 5 V	V_5V
	V_{OUT}	3.57…3.75 V	V_3V6_10G
	I_{OUT}	max. 1.5 A	Peak
V_3V3A_10G	V_{IN}	typ. 3.6 V	V_3V6_10G
	V_{OUT}	3.262…3.338 V	V_3V3A_10G
	I_{OUT}	max. 1.5 A max. 0.8 A	Peak Average

3.27.7 V_1V05

The voltage required for the Ethernet PHYs and the USB 3.0 hub is generated from V_3V3.

Table 36: Specification V_1V0_ETH

Voltage	Parameter	Value	Remark
V_1V05	V_{IN}	typ. 3.3 V	V_3V3
	V_{OUT}	1.057…1.089 V	V_1V05
	I_{OUT}	1.5 A	Load: max. 909 mA

3.27.8 V_2V5_ETH

The Ethernet PHYs need among others a supply of 2.5 V, which is generated for both PHYs from V_3V3. The supply of the PHYs is thus automatically started after the boot process.

Table 37: Specification V_2V5_ETH

Voltage	Parameter	Value	Remark
V_2V5_ETH	V_{IN}	typ. 3.3 V	V_3V3
	V_{OUT}	2.44…2.56 V	V_2V5_ETH
	I_{OUT}	320 mA	Load: max. 170 mA

3.27.9 V_12V

A voltage of 12 V is required for the backlight supply at the LVDS, the fan as well as the starter kit pin header, which is specified with 2.5 A in total. The voltage is generated from V_24V by a step-down converter. The controller can be switched on or off via GPIO signal by software.
The design has the following specification:

Table 38: Specification V_12V

Voltage	Parameter	Value	Remark
V_12V	V_{IN}	16…32 V	V_24V
	V_{OUT}	11.660…12.471 V	V_12V
	I_{OUT}	2.5 A	

3.28 Reset & Configuration

Figure 28 shows the reset structure on the MBa95xxCA.
In addition to the reset signals of the TQMa95xxLA, the MBa95xxCA also provides further software-controlled reset signals for individual function blocks, e.g. ENET reset for the Ethernet transceivers.

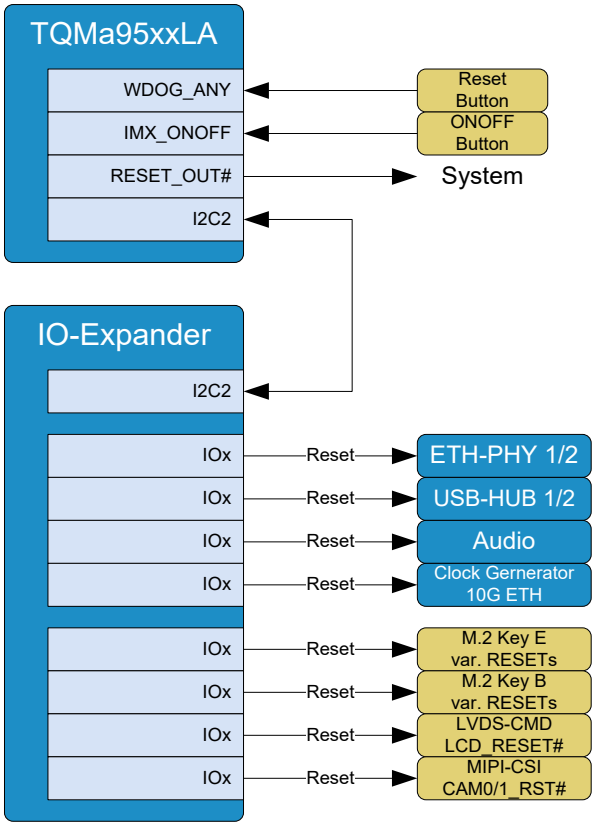


Figure 27: Block diagram Reset & Configuration

The following signals from the TQMa95xxLA are used on the MBa95xxCA:

Table 39: Reset signals

Signal	Type	Level	Remark
WDOG_ANY#	I	3.3 V	• activates RESET of the PMIC (low-active) • no pull-up on mainboard necessary • connect to GND for activation (push button)
RESET_OUT#	O	-	• open drain output (low-active) • activates RESET of mainboard components • requires pull-up on mainboard (max. 5.5 V)
IMX_ONOFF	I	1.8 V	• ON/OFF function of the i.MX95 (see data sheet) • no pull-up on mainboard necessary • connect to GND to activate (push button)

Pushbuttons are connected to WDOG_ANY# and IMX_ONOFF.
RESET_OUT is connected with a pull-up to V_3V3 and resets followed blocks:

- IO Expander
- Analog switch for boot mode signals
- External components at starter kit headers

The reset signal is linked to an LED.

4. SOFTWARE

No software is required for the MBa95xxCA.
Suitable software is only required on the TQMa95xxLA and is not a part of this User's Manual.
More information can be found in the TQ-Support Wiki for the TQMa95xx.

5. MECHANICS

5.1 MBa95xxCA dimensions

The MBa95xxCA has overall dimensions (length × width × height) of 170 mm × 170 mm × TBD mm.
The MBa95xxCA has six 4.2 mm mounting holes for the housing, and four 2.7 mm mounting holes for a heat sink.
The MBa95xxCA weighs approximately TBD grams without TQMa95xxLA.

5.2 Embedding in the target system

The MBa95xxCA serves as a design base for customer products, as well as a reference platform during development.

5.3 Housing

The form factor and the mounting holes of the MBa95xxCA are designed for installation in a standard Mini-ITX housing.

5.4 Thermal management

The largest power dissipation on the MBa95xxCA is caused by the voltage regulators. In addition, the TQMa95xxLA is a heat source that acts indirectly on the MBa95xxCA. Depending on the application, further power dissipation can occur, mainly at additional external loads on the pin headers on the MBa95xxCA, the M.2 slots, etc.
For evaluation of the TQMa95xxLA under high load conditions an optional heat sink is provided. Four holes are provided on the MBa95xxCA for this purpose. A connector is available on the MBa95xxCA for connecting an optional fan.

Attention: TQMa95xxLA heat dissipation	
	The i.MX 95 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa95xxLA must be taken into consideration when connecting the heat sink. The TQMa95xxLA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa95xxLA or the MBa95xxCA and thus malfunction, deterioration or destruction.

5.5 Assembly & Labels

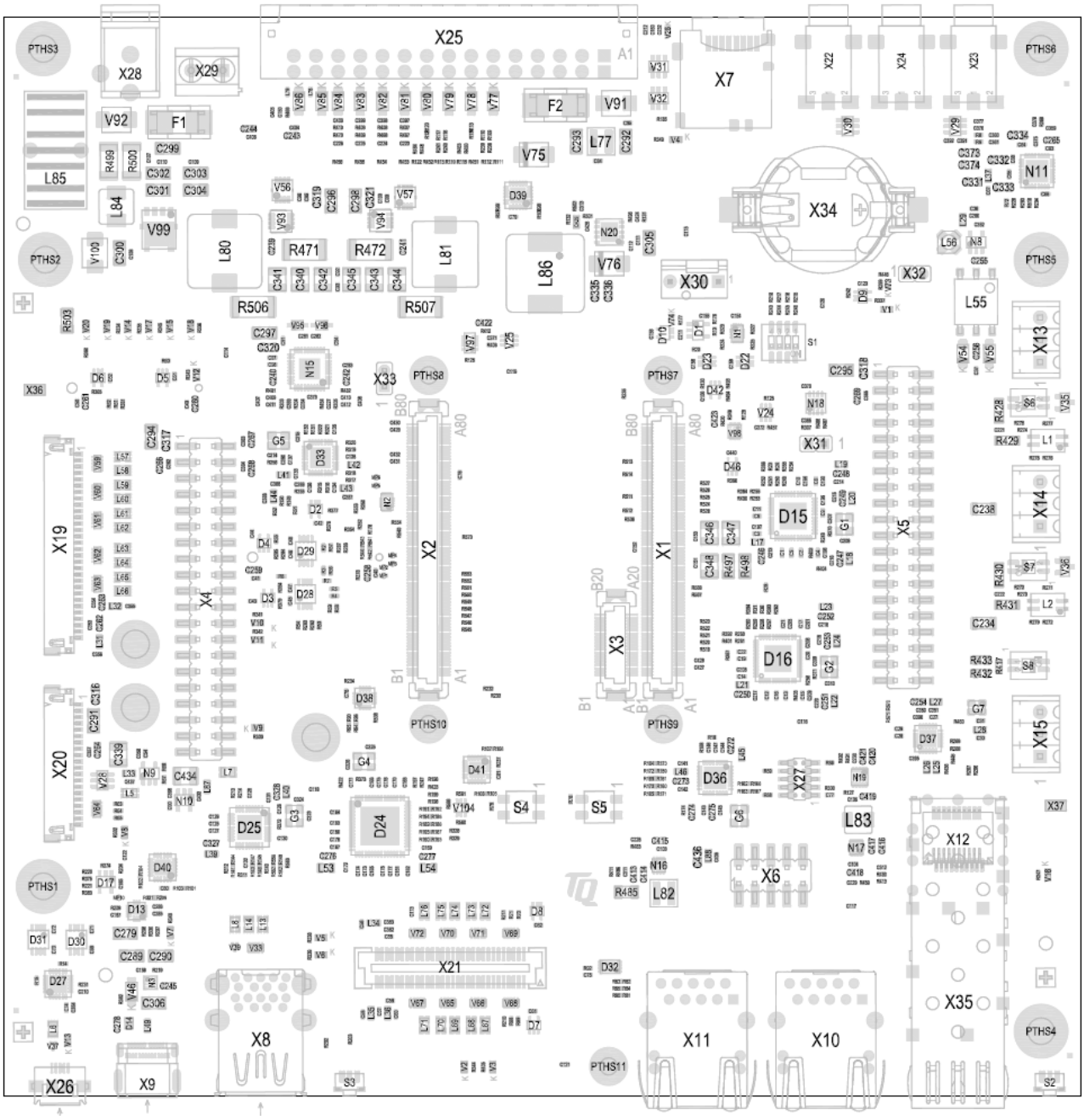


Figure 28: MBa95xxCA top view

The labels on the MBa95xxCA show the following information:

Table 40: Labels on MBa95xxCA

Label	Content
AK1	TBD
AK2	TBD

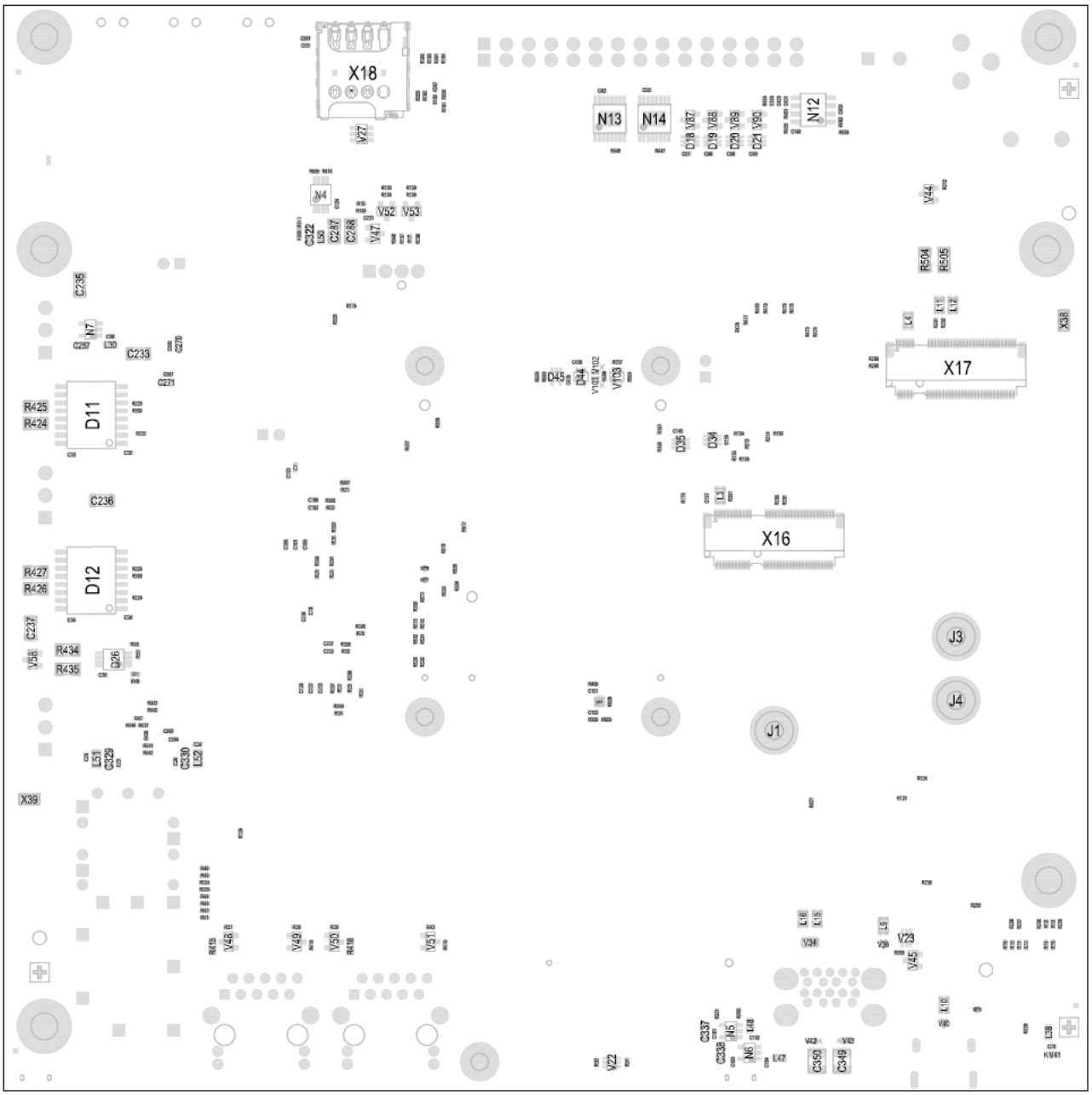


Figure 29: MBa95xxCA bottom view

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Since the MBa95xxCA is a development platform, no EMC tests have been performed.
During the development of the MBa95xxCA the standard DIN EN 55022:2010 limit class A was taken into account.

6.2 ESD

ESD protection is provided on most interfaces of the MBa95xxCA.
The MBa95xxCA schematics show, which interfaces provide ESD protection.

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤32 V DC.

6.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the MBa95xxCA is only a sub-component of an overall system.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 41: Climatic and operational conditions MBa95xxCA

Parameter	Range	Remark
Ambient temperature	–25 °C to +85 °C	
Storage temperature	–40 °C to +100 °C	
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMa95xxLA heat dissipation	
	The i.MX 95 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa95xxLA must be taken into consideration when connecting the heat sink. The TQMa95xxLA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa95xxLA and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBa95xxCA. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa95xxCA.

The MBa95xxCA is designed to be insensitive to vibration and impact.

7.3 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

7.4 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa95xxCA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa95xxCA was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa95xxCA must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBa95xxCA enable compliance with EuP requirements for the MBa95xxCA.

8.5 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.
The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.
Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.
TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

8.6 Packaging

The MBa95xxCA is delivered in reusable packaging.

8.7 Batteries

8.7.1 General notes

For technical reasons a battery is necessary for the MBa95xxCA. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.7.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa95xxCA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa95xxCA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 42: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AI	Analog Input
ARM®	Advanced RISC Machine
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CLC	Capacitor-Inductor-Capacitor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3L	Double Data Rate 3 Low voltage
DIN	Deutsche Industrienorm (German industry standard)
DIP	Dual In-line Package
DSI	Display Serial Interface
eCSPI	enhanced Capability Serial Peripheral Interface
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European Standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FET	Field Effect Transistor
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communication
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IP00	Ingress Protection 00
I_{PD}	Input with Pull-Down
I_{PU}	Input with Pull-Up
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean (operating) Time Between Failures

9.1 Acronyms and definitions (continued)

Table 39: Acronyms (continued)

Acronym	Meaning
NAND	Not-And (flash memory)
(NC)	Not Connected
NOR	Not-Or
NP	Not Placed
O_{OD}	Open-Drain Output
O_{PD}	Output with Pull-Down
O_{PU}	Output with Pull-Up
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PD	Pull-Down
PHY	Physical (Interface)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial Gigabit Media-Independent Interface
SIM	Subscriber Identification Module
SMI	Serial Management Interface
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
UIM	User Identity Module
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 43: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX95 Industrial Application Processors Data Sheet	2, June 2024	NXP
(2)	i.MX95 Hardware Developer's Guide	B, 07.05.2024	NXP
(3)	i.MX 95 – Reference Manual	TBD	NXP
(4)	i.MX 95 – Mask Set Errata	TBD	NXP
(5)	Ethernet Transceiver DP83867– Application Report	October 2015	TI
(6)	TQMa95xxLA User's Manual	– current –	TQ-Systems
(7)	TQMa95xxLA Support Wiki	– current –	TQ-Systems

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