MBa8MPxL
User's Manual

MBa8MPxL UM 0102
29.05.2024

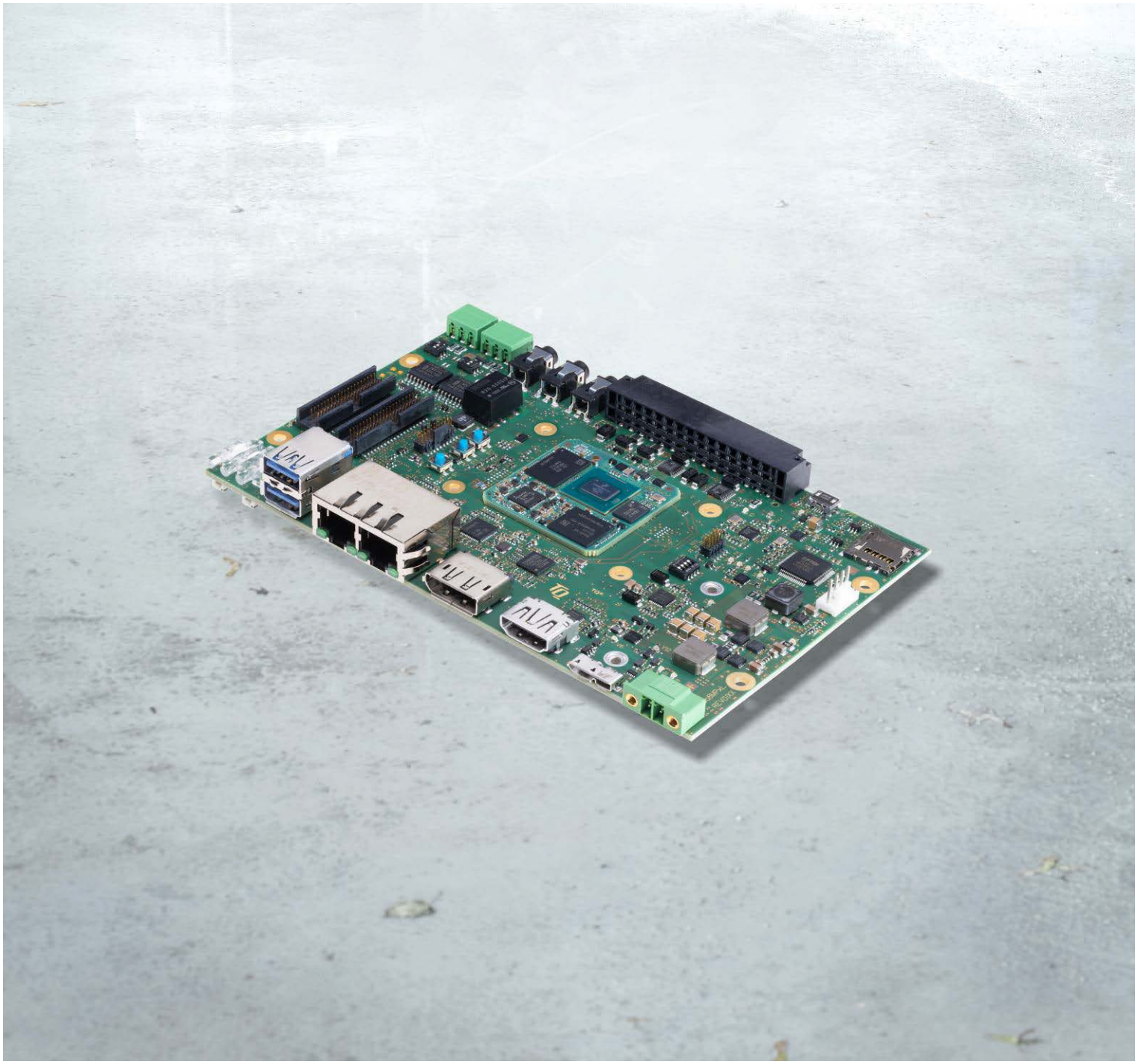

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TABLE DIRECTORY

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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	06.03.2021	Petz		First edition
0002	16.03.2021	Petz	All Figure 1 Table 2 Table 22, Table 23, Table 24 5.1 Figure 24	Non-functional changes, expressions, phrases Updated “3.3 V” for X555 removed “Level” and “Dir.” for 1.8 V, 3.3 V, and 5 V added Weight corrected (147 grams ⇨ 143 grams) Corrected
0100	04.08.2022	Kreuzer	All	Update to board revision 02xx and 03xx
0101	16.09.2022	Kreuzer	Figure 4 Figure 5 3.1.3 Figure 9 Table 19	TPM added Presentation simplified for better clarity Assembly options added PHY numbering corrected Tolerance change of the 24 V voltages to ± 10 %
0102	29.05.2024	Kreuzer	3.4.2 6.4, 6.5, 6.6, 6.7, 8.4	Assembly options clarified Chapter added

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa8MPxL and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required for full comprehension of this User's Manual:

- MBa8MPxL schematics
- TQMa8MPxL User's Manual
- i.MX 8M Plus Data Sheet
- i.MX 8M Plus Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: https://support.tq-group.com/en/layerscape/tqma8mpxl

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBa8MPxL as of revision 02xx and 03xx.

The MBa8MPxL is designed as a carrier board for the TQMa8MPxL. The TQMa8MPxL is directly soldered on the MBa8MPxL.

Core of the MBa8MPxL is the TQMa8MPxL with an NXP i.MX 8M Plus CPU based on a Dual or Quad Cortex®-A53.

The TQMa8MPxL connects all peripheral components. In addition to the standard communication interfaces such as USB, Ethernet, SD card, etc., most other available TQMa8MPxL signals are routed on 50 mil pin headers on the MBa8MPxL.

CPU features and interface can be evaluated, software development for a TQMa8MPxL-based project can start immediately.

Currently four i.MX 8M Plus derivatives are supported:

1) i.MX 8M Plus Dual (Dual Cortex®-A53)
2) i.MX 8M Plus Quad 4 Lite (Quad Cortex®-A53)
3) i.MX 8M Plus Quad 6 Video (Quad Cortex®-A53)
4) i.MX 8M Plus Quad 8 ML/AI (Quad Cortex®-A53)

2.1 MBa8MPxL block diagram

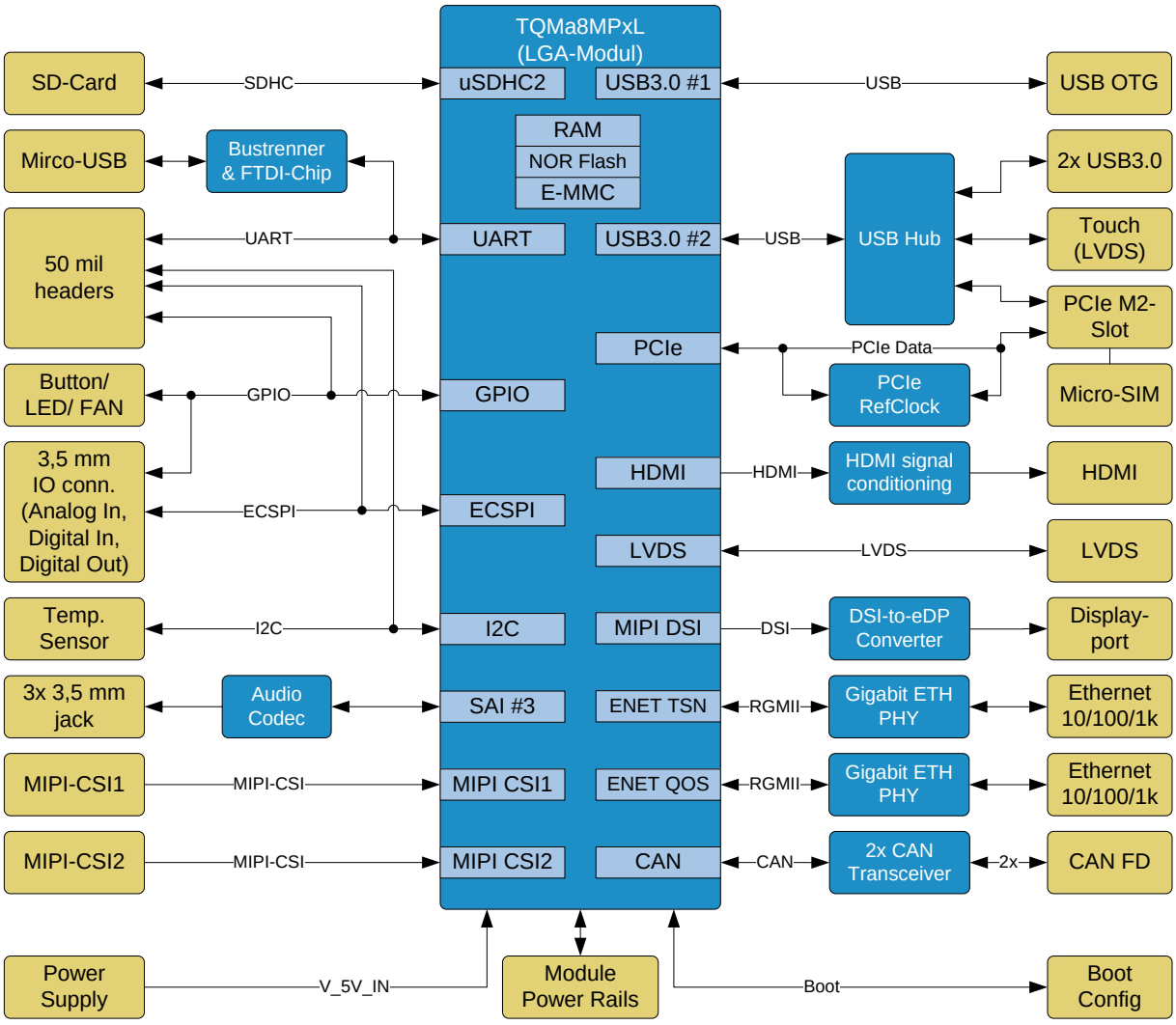

Figure 1: Block diagram MBa8MPxL

2.2 MBa8MPxL interfaces, overview

The following interfaces/functions and user interfaces are available on the MBa8MPxL:

Table 2: Data interfaces

Interface	Connector	Type	Remark
Audio	X15, X16, X17	3 × 3.5 mm jack	MIC (mono), Line-in (stereo), Line-out (stereo)
CAN FD	X18, X19	MC 1,5/ 3-G-3,5	X18: CAN0 | X19: CAN1
eDP / DP	X65	DisplayPort	DSI-to-DP bridge
Eth 1000 Base-T	X66	Double RJ45	Gigabit PHY DP83867 and socket with integrated transformers
GPIO / ADC	X555	DMC 1,5/15-G1F-3,5-LR P20THR	Connected to IO bank, usage up to 24 V (GPIO)
HDMI	X44	HDMI	–
I^2C	X61	40-pin, 50 mil pin header	4 × I^2C
JTAG	X22	10-pin, 50 mil pin header	JTAG
LVDS CMD	X7	20-pin, DF19G	ZIF connector + USB 2.0
LVDS Data	X11	30-pin, DF19G	ZIF connector
MIPI CSI	X57	60-pin, 0.8 mm, TE Connectivity	CSI1 and CSI2
PCIe / M.2	X48	M.2	PCIe + USB 2.0
SIM card	X46	SIM card holder	SIM card slot
SD card	X42	USDHC2	Optional boot source and supply of module
USB 3.0	X36	Stacked Type A	USB 3.0 H1, top, USB 3.0 H2, bot
USB 3.0 OTG	X29	USB1-Interface at USB Micro-B	USB OTG or Serial Download Mode
USB Debug	X28	UART3, UART4	Via FTDI chip to micro USB AB socket

The MBa8MPxL provides the following diagnostic and user interfaces:

Table 3: Diagnostic and user interfaces

Interface	Reference	Component	Remark
Status LEDs		1 × Red LED	Reset
		7 × Green LED	Voltages on MBa8MPxL
		2 × Green LED	General purpose LEDs
		3 × Orange LED	V_3V3_MOD, V_3V3_SD, V_1V8_MOD
		1 × Yellow LED	General purpose LED
Temperature sensor	D1	1 × SE97BTP	Digital I^2C temperature sensor
Power / Reset	S7 S8 S9	3 × Pushbutton	Reset PMIC reset CPU-ON/OFF
GP button	S12, S13	2 × Pushbutton	General purpose pushbuttons
Boot-Mode	S1	1 × 4-fold DIP switch	Boot Device selection
Coin cell	X56	1 × battery socket	Standard CR2032, RTC buffer

2.3 MBa8MPxL interfaces, location

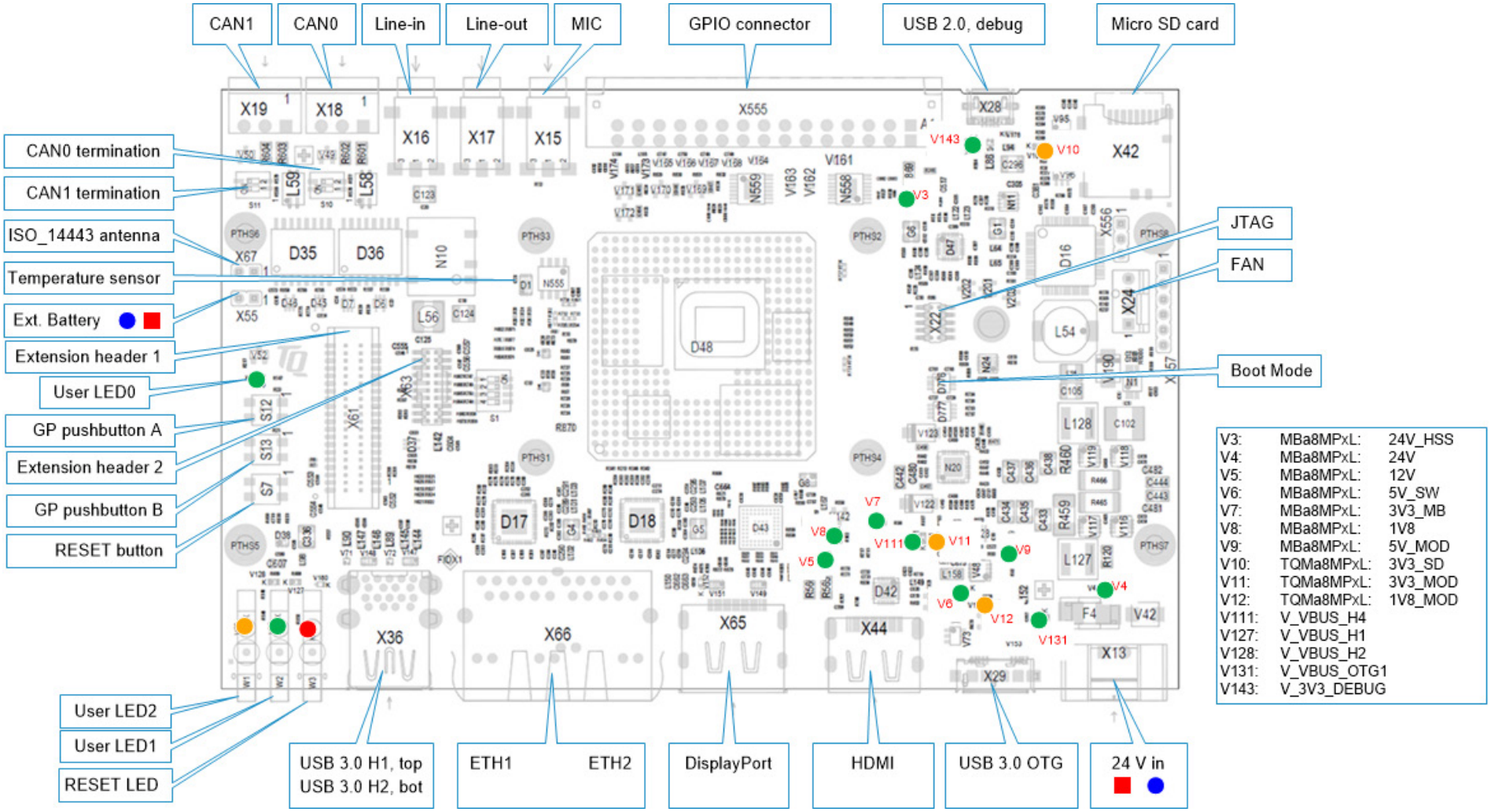

Figure 2: MBa8MPxL interfaces top

2.3 MBa8MPxL interfaces, (continued)

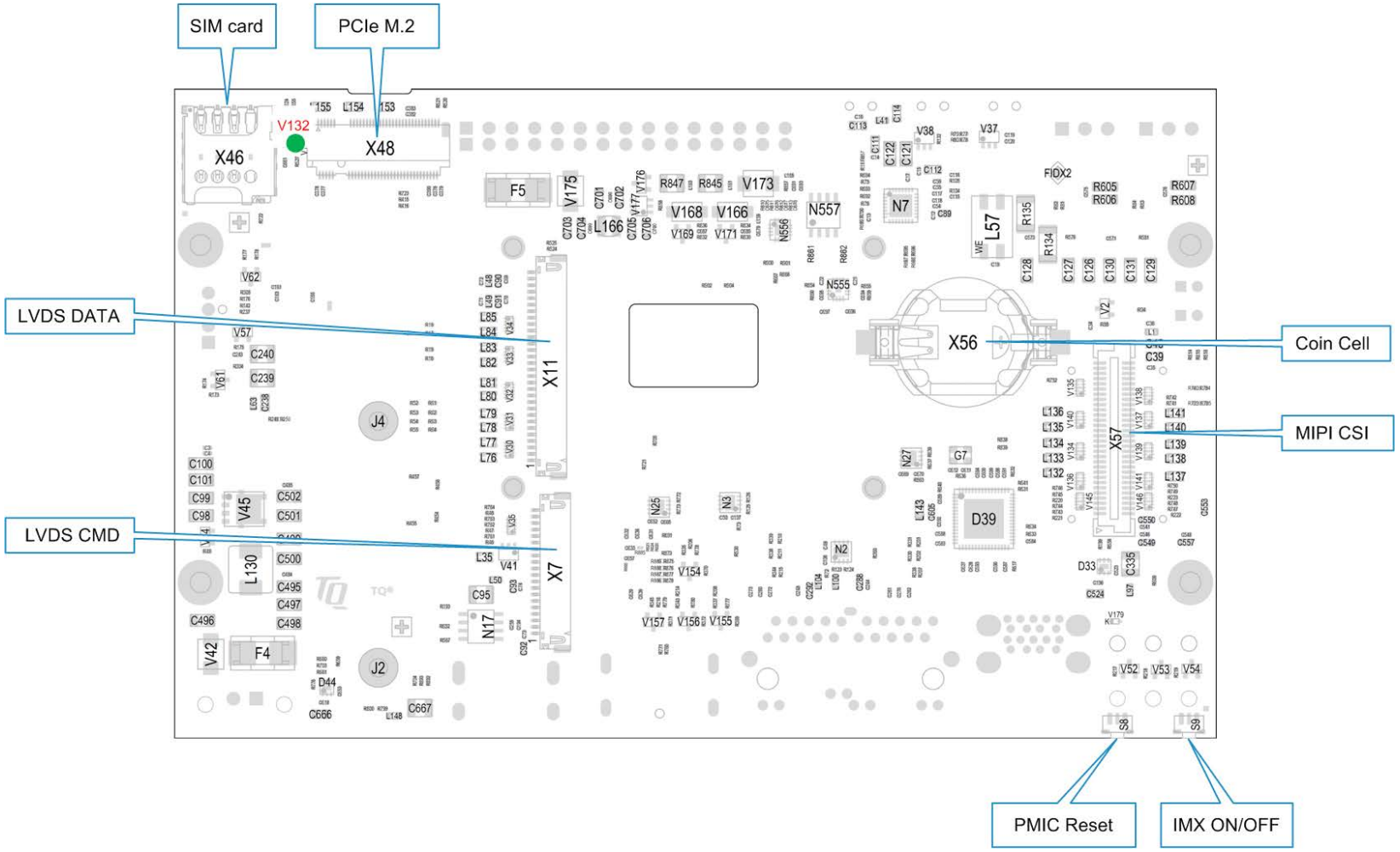

Figure 3: MBa8MPxL interfaces bottom

3. ELECTRONICS

3.1 MBa8MPxL functional groups

The following chapters describe the interfaces of the MBa8MPxL in connection with a TQMa8MPxL.

3.1.1 TQMa8MPxL overview

The MBa8MPxL provides all power supplies and configurations required for the operation of the TQMa8MPxL.
The TQMa8MPxL is the central system on the MBa8MPxL. It provides LPDDR4 SDRAM, eMMC, NOR flash, RTC, an EEPROM, power supply and power management functionality. All TQMa8MPxL internal voltages are derived from the 5 V supply voltage.
All functionally relevant pins of the i.MX 8M Plus are routed to the TQMa8MPxL connectors or LGA pads. This enables to use the TQMa8MPxL with all the freedom that comes with a customer-specific design-in solution. Further information can be found in the TQMa8MPxL User's Manual.
On the MBa8MPxL the standard interfaces like USB, Ethernet, etc., provided by the TQMa8MPxL are routed to industry standard connectors. All other relevant signals and buses provided by the TQMa8MPxL are routed to 50 mil pin headers on the MBa8MPxL.
The boot behaviour of the TQMa8MPxL can be controlled. The boot mode configuration is set with a DIP switch on the MBa8MPxL.

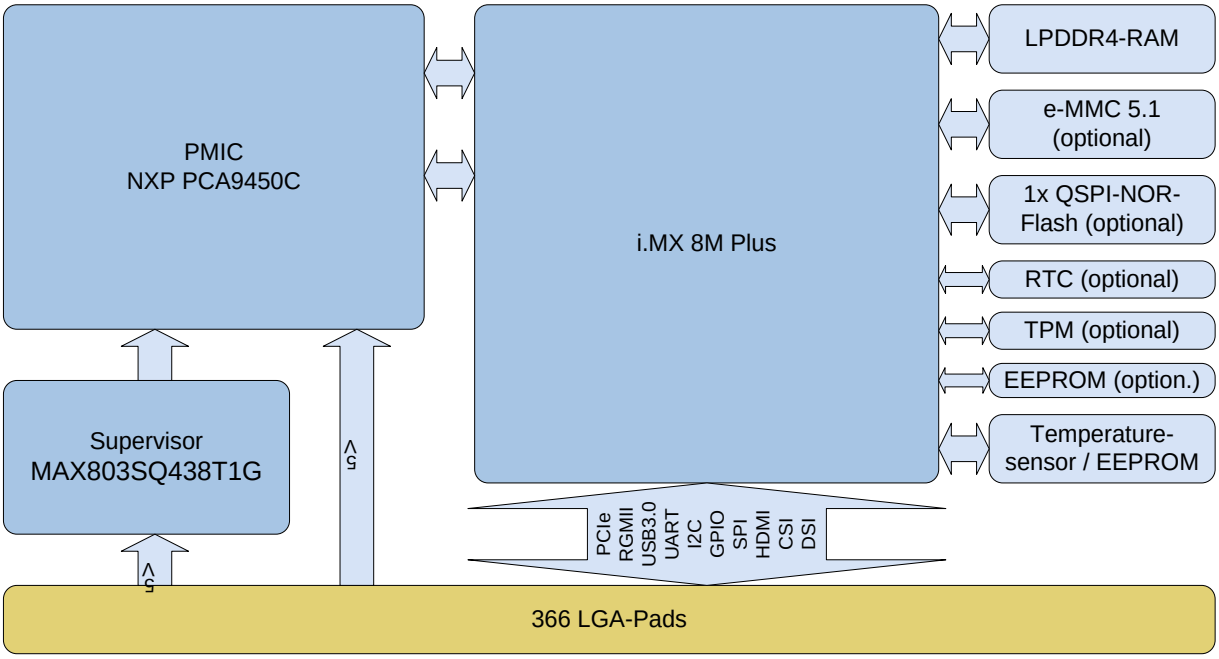

Figure 4: Block diagram TQMa8MPxL

3.1.2 TQMa8MPxL pinout

All relevant TQMa8MPxL signals are routed to 50 mil pin headers on the MBa8MPxL.

Note: Available interfaces	
	Depending on the TQMa8MPxL derivative, not all interfaces are available. More information about available interfaces can be found in the TQMa8MPxL User's Manual and pinout tables.

3.1.3 I²C devices, address mapping

The TQMa8MPxL provides four I²C buses. Of these, only I2C6 is provided on a pin header. All other buses are used by different components on the module or the mainboard.

Per assembly option I2C1 or I2C6 can be connected to the bus I2C_3V3 instead of I2C2. Per assembly option I2C2_1V8 can be connected to the MIPI_CSI connector instead of I2C4_1V8.

All I2C buses provided by the TQMa8MPxL have a 3.3 V level. In order to be able to connect 1.8 V components as well, two level converters are used on the MBa8MPxL. One is permanently connected to I2C4, the second can be varied in its connection, but uses I2C2 by default.

The following block diagram shows the I²C bus structure.

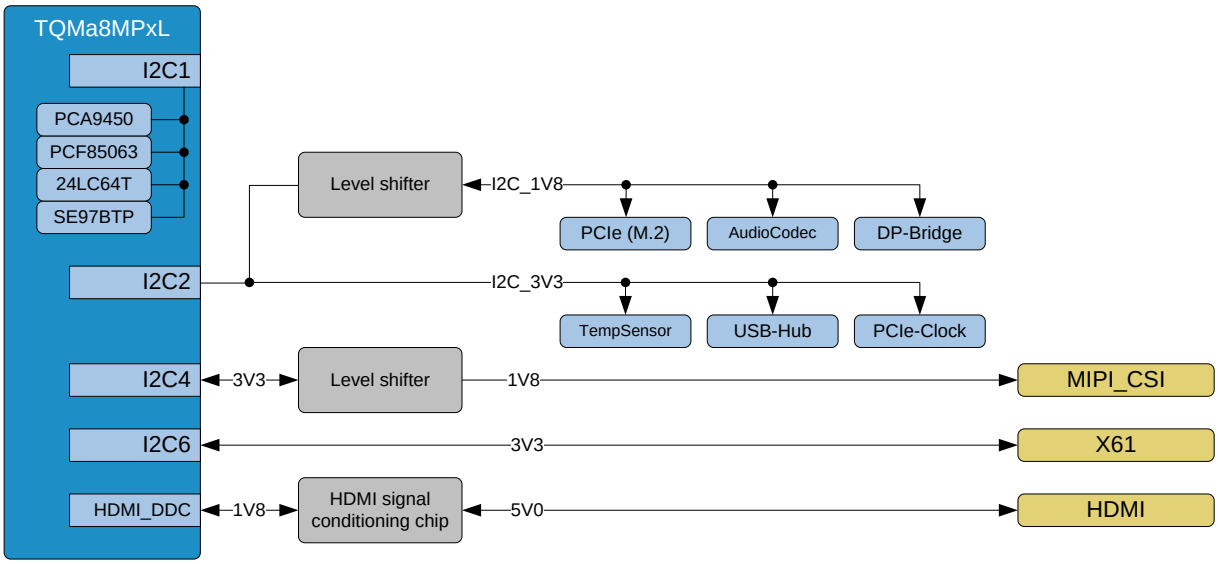

Figure 5: Block diagram I²C bus

The following table shows the addresses used on the TQMa8MPxL and the MBa8MPxL.

Table 4: I²C devices, address mapping on TQMa8MPxL and MBa8MPxL

Location	Device	Function	7-bit address	Remark
TQMa8MPxL	PCA9450	System Controller	0x25 / 010 0101b	Should not be altered
	PCF85063	RTC	0x51 / 101 0001b	Optional
	24LC64T	EEPROM	0x57 / 101 0111b	Optional
	SE97BTP	Temperature sensor	0x1B / 001 1011b	–
		EEPROM	0x33 / 011 0011b	R/W access in Protected Mode
			0x53 / 101 0011b	R/W access in Normal Mode
	SE050	Trust Secure Element	0x48 / 100 1000b	Optional
MBa8MPxL	TLV320AIC3204	Audio Codec	0x18 / 001 1000b	N7
	SE97B	Temperature sensor	0x1C / 001 1100b	D1
		EEPROM	0x34 / 011 0100b	D1, R/W access in Protected Mode
			0x54 / 101 0100b	D1, R/W access in Normal Mode
	TUSB8041	USB 3.0 Hub	0x44 / 100 0100b	D39, optional, not connected
	9FGV0441A	PCIe Clock Generator	0x6A / 110 1010b	D47
	TC9595XBG	MIPI DSI to DP	0x0F / 000 1111b	D43
	Socket	PCIe M.2	(Device dependent)	X48

3.1.4 RTC backup

In case of power failure or power down, a lithium battery type CR2032 on the MBa8MPxL supplies the RTC on the TQMa8MPxL, which can be supplied with 2.1 V to 3.7 V, typical 3.0 V. The TQMa8MPxL features an i.MX 8M Plus-internal RTC or a discrete RTC PCF85063A. The RTC is supplied in either way.

3.1.5 Temperature sensor

For temperature monitoring on the TQMa8MPxL and the MBa8MPxL, there is one SE97BTP sensor each.

The sensors are connected to I2C1; see Table 4. The I^2C address of the sensor on the MBa8MPxL can be adapted by rearranging 0 Ω bridges. When changing the address, care must be taken to avoid address conflicts with existing I^2C devices.

The assembly options are documented in the MBa8MPxL schematics.

The temperature sensor D1 is located on the top side of the MBa8MPxL; see Figure 2.

Table 5: Temperature sensor SE97BTP, D1

Manufacturer	Device	Resolution	Accuracy	Temperature range
NXP	SE97BTP	11 bits	Max. ±1 °C	+75 °C to +95 °C
			Max. ±2 °C	+40 °C to +125 °C
			Max. ±3 °C	–40 °C to +125 °C

3.1.6 Fan

Depending on the load of the CPU and other module components, it may be necessary to use a fan for active cooling in addition to the use of a heat sink. A corresponding circuit is provided on the MBa8MPxL.

The RPM signal of the fan is connected to GPT2_CLK, the PWM signal for speed control to PWM3. Both are 3.3 V signals.

The FAN PWR signal for switching the fan is connected to the module as 1.8 V GPIO signal GPIO4_IO27.

Table 6: Pinout fan connector, X24

Pin	Signal	Remark
1	DGND	–
2	V_FAN	12 V via R249 on MBa8MPxL (default), optional 5 V via R250 on MBa8MPxL
3	RPM	GPT2_CLK of TQMa8MPxL, 3.3 V
4	PWM	PWM3 of TQMa8MPxL, 3.3 V

3.1.7 Reset

The RESET_OUT# signal of the TQMa8MPxL is available on the MBa8MPxL.
A red LED (V59) on the MBa8MPxL indicates a reset condition; see Table 26.
On the MBa8MPxL a partial reset of the TQMa8MPxL is possible, e.g. with signals PMIC_WDOG_IN# and RESET_IN#.

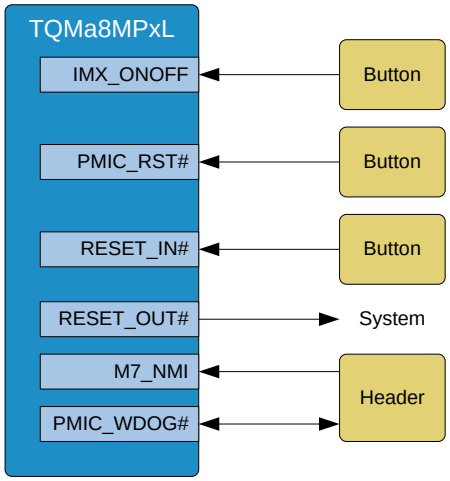

Figure 6: Block diagram MBa8MPxL Reset structure

Attention: RESET_OUT# / PMIC_RST#	
	Attention: The signal RESET_OUT# is designed as a reset triggering signal. To feed a reset signal into the system, it is mandatory to use the signal PMIC_RST#.

Table 7: Reset signals

Signal	Dir.	Source	Default	Remark
RESET_OUT#	O	TQMa8MPxL	High	• Open drain output; low-active • Activates RESET of MBa8MPxL components • Requires pull-up on carrier board (max. 6.5 V)
RESET_3V3#	O	MBa8MPxL	High	• Generated on MBa8MPxL from RESET_OUT#
IMX_ONOFF	I	MBa8MPxL	High	• ON/OFF function; see i.MX 8M Plus data sheet (1) • No pull-up on carrier board required; low-active • Connect 5 s to GND to activate
PMIC_RST#	I	MBa8MPxL	High	• No pull-up on carrier board required; low-active • Programmable PMIC response (warm reset, cold reset)
RESET_IN#	I	MBa8MPxL	High	• Activates POR_B of the i.MX 8M Plus; low-active • Connect to GND to activate
M7_NMI	I	MBa8MPxL	High	• Multiplexed to GPIO1_IO05 pin of i.MX 8M Plus • Interrupt signal for M7 Sub-CPU with defined priority
PMIC_WDOG_IN#	I	MBa8MPxL	High	• No pull-up on carrier board required; low-active • Disabled by default on PMIC side • Programmable PMIC response (warm reset, cold reset)
PMIC_WDOG_OUT#	O	TQMa8MPxL	–	• Multiplexed to GPIO1_IO02 pin of i.MX 8M Plus • Connected to PMIC_WDOG_IN# via 0 Ω bridge

3.2 Power supply

At X13, the MBa8MPxL has to be supplied with 24 V +10 % / –33 % (16 V to 26.4 V). All other voltages required on the MBa8MPxL are derived from the supply voltage. 5 V (2.2 A), 3.3 V (1.75 A) and 1.8 V (0.75 A) are available at pin headers X61 and X63. It must be ensured that the permissible limit values of the input circuitry are not exceeded.

The MBa8MPxL has a theoretical maximum power consumption of approx. 158.4 W at its 24 V supply connection. This corresponds to a maximum typical current of 6.6 A at 24 V. The power supply unit used must be selected accordingly. In most applications, however, the power consumption will be significantly lower and the MBa8MPxL including TQMa8MPxL consumes approx. 5 W to 6 W when the i.MX 8M Plus operates at 100 % load. Most of the theoretically possible power consumption results from the standard-compliant supply of the USB, PCIe (M.2) and LVDS interfaces, as well as from the power available at the pin headers.

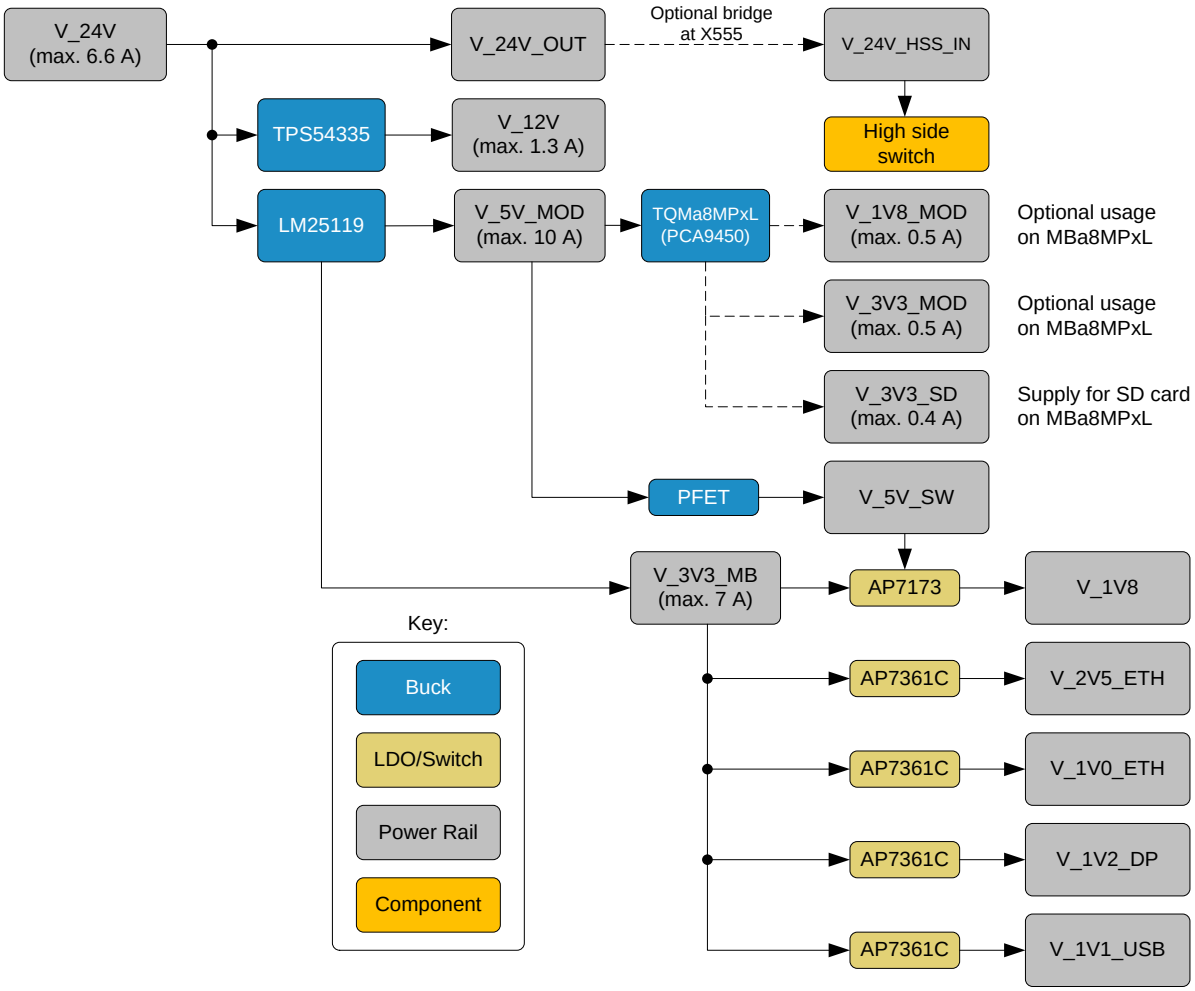

Figure 7: Block diagram power supply MBa8MPxL

3.2.1 Protective circuitry

The protective circuit (see Figure 8) features the following characteristics:

- Overcurrent protection by fuse 7 A, Slow Blow
- Overvoltage protection
- PI filter
- Reverse polarity protection
- Capacitors for voltage smoothing

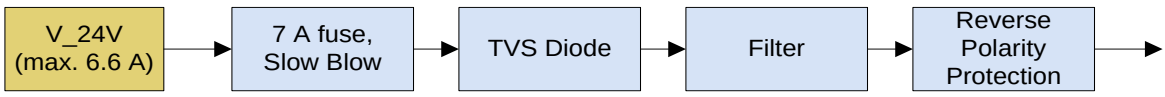

Figure 8: MBa8MPxL protective circuit

3.3 Communication interfaces

3.3.1 Ethernet 1000 Base-T (RGMII)

The i.MX 8M Plus CPU has two independent RGMII interfaces. On the MBa8MPxL both interfaces are used to provide two Gigabit Ethernet ports by means of two DP83867 Ethernet PHYs.

The PHY has boot straps to start with adjustable default values. Some boot straps can be customized with placement options. More information is available in the latest MBa8MPxL schematic.

Both interfaces additionally provide event signals according to IEEE 1588, which can be used to realize high precision synchronizations between Ethernet components. These signals are available from ENET0 at X63 by default. If required, the event signals of ENET1 can be used via assembly option.

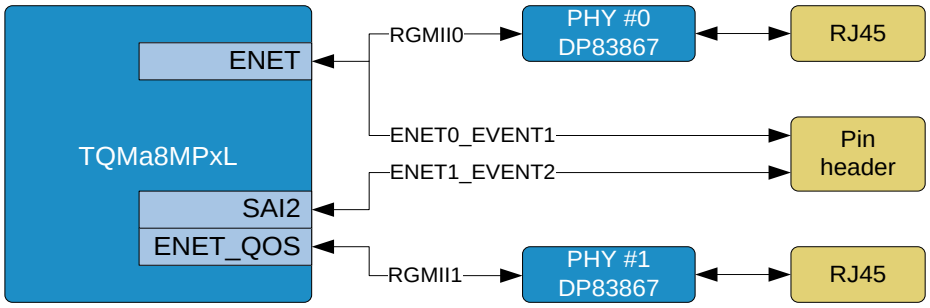

Figure 9: Block diagram Ethernet 1000 Base-T

Table 8: Pinout RJ45 Ethernet connector, X66

X66, left RJ45			X66, right RJ45			Remark
Pin	Pin name	Signal	Pin	Pin name	Signal	
1A	GND	GND	1B	GND	GND	–
2A	TD0+	ENET0_A+	2B	TD0+	ENET1_A+	–
3A	TD0–	ENET0_A–	3B	TD0–	ENET1_A–	–
6A	TD1+	ENET0_B+	6B	TD1+	ENET1_B+	–
4A	TD1–	ENET0_B–	4B	TD1–	ENET1_B–	–
5A	TD2+	ENET0_C+	5B	TD2+	ENET1_C+	–
7A	TD2–	ENET0_C–	7B	TD2–	ENET1_C–	–
8A	TD3+	ENET0_D+	8B	TD3+	ENET1_D+	–
9A	TD4–	ENET0_D–	9B	TD4–	ENET1_D–	–
10A	CHS.GND	GND	10B	CHS.GND	GND	–
11A	GREEN_ANODE	V_3V3_MB	11B	GREEN_ANODE	V_3V3_MB	120 Ω in series
12A	GREEN_CATHODE	ENET0_LED_0	12B	GREEN_CATHODE	ENET1_LED_0	Switched by transistor
13A	YELLOW_ANODE	V_3V3_MB	13B	YELLOW_ANODE	V_3V3_MB	120 Ω in series
14A	YELLOW_CATHODE	ENET0_LED_2	14B	YELLOW_CATHODE	ENET1_LED_2	Switched by transistor

3.3.2 SD card interface

The MBa8MPxL offers a microSD card slot that can also be used as boot source. All signals are directly connected to the USDHC2 interface of the i.MX 8M Plus.

The TQMa8MPxL voltage V_3V3_SD supplies the microSD card slot. Since this voltage is controlled by SD_RESET#, the microSD card is automatically reset in case of a Reset. An external switch is not required. Signal USDHC2_CD# has a pull-up on the MBa8MPxL. All data lines are ESD protected.

Standard, High and Extended capacity card types are supported. Default Speed, High Speed, and SD UHS-1 Speed Mode SDR104 with theoretically max.104 MB/s are supported. UHS-1 Speed Modes SDR12, SDR25, SDR50 and DDR50 are theoretically supported but not verified.

The TQMa8MPxL sets USDHC2 is to 1.8 V or 3.3 V automatically, depending on the transfer mode. The corresponding driver handles the changeover; it does not have to be done explicitly.

USDHC2_WP is not used and is terminated accordingly.

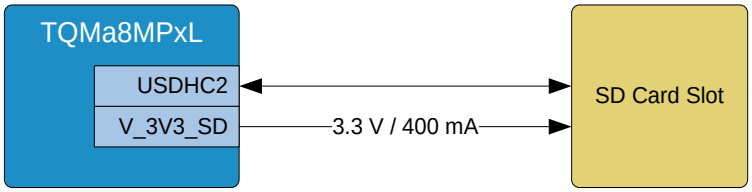

Figure 10: Block diagram SD card interface, MBa8MPxL

Table 9: Pinout microSD card, X42

Pin	Pin name	Signal	Remark
1	DAT2	USDHC2_DATA2	10 kΩ PU
2	DAT3	USDHC2_DATA3	10 kΩ PU
3	CMD	USDHC2_CMD	10 kΩ PU
4	VDD	V_3V3_SD	Supply from TQMa8MPxL
5	CLK	USDHC2_CLK	–
6	GND	GND	–
7	DAT0	USDHC2_DATA0	10 kΩ PU
8	DAT1	USDHC2_DATA1	10 kΩ PU
SW1	CD#	GND	–
SW2	CD#	USDHC2_CD#	10 kΩ PU
M1…4	Shield	GND	–

3.3.3 USB 3.0 Hub

A USB 3.0 hub TUSB8041 is connected to the USB2 interface on the MBa8MPxL, which provides four USB 3.0 / 2.0 host interfaces.

USB Host 1 & 2 of the TUSB8041 are connected to a Dual USB 3.0 Type A socket (X36) on the MBa8MPxL. USB Host 3 is routed to the PCIe M.2 connector X48, USB Host 4 is routed to the LVDS-CMD connector X7 on the MBa8MPxL.

The USB hub is programmed via bootstrapping or I²C. Further information can be found in the TUSB8041 data sheet and the MBa8MPxL schematics.

The USB connectors are supplied with 5 V via power switches. The current is monitored and can be switched off in case of an overload and/or overheating.

The USB 3.0 port of the TQMa8MPxL provides a theoretical data rate of 5 Gbit/s. This is divided among the connected ports on the MBa8MPxL. Depending on the software and hardware used, the effective read and write rates of the ports may vary.

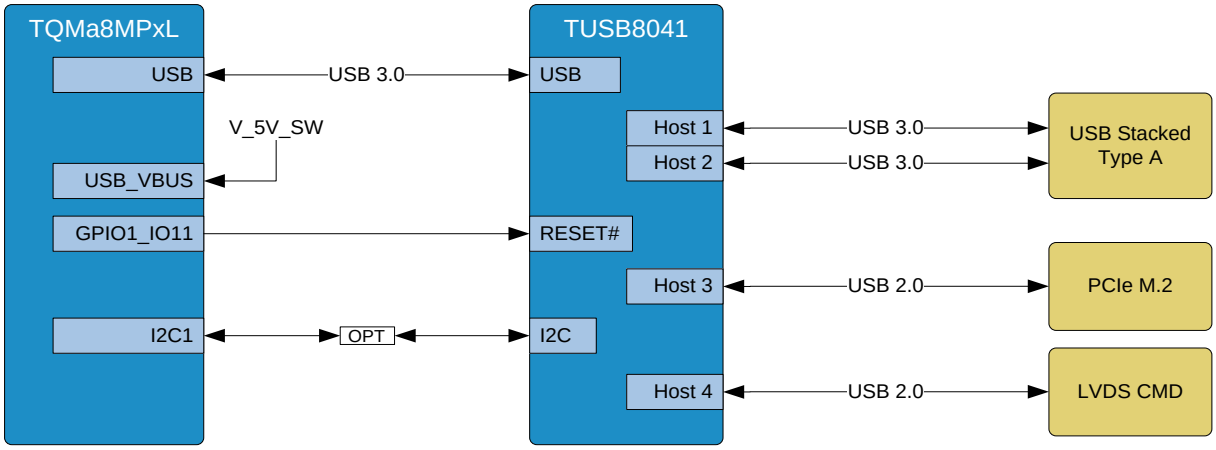

Figure 11: Block diagram USB 3.0 Hub

3.3.4 USB 3.0 OTG

The second TQMa8MPxL USB interface is configured as USB 3.0 OTG and routed to USB Micro-B connector X29 on the MBa8MPxL.

This interface can be used for the Serial Download Mode of the TQMa8MPxL. It can be used as a normal USB 3.0 or USB 2.0 interface via an adapter.

The USB connector is supplied with 5 V via a power switch. The current is monitored and can be switched off in case of an overload and/or overheating.

The USB1 port of the TQMa8MPxL provides a theoretical data rate of 5 Gbit/s. Depending on the software and hardware used, the effective read and write rates of the ports may vary.

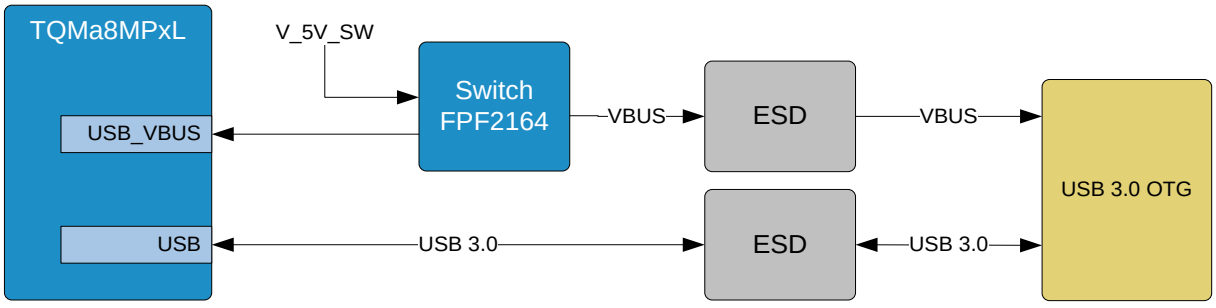

Figure 12: Block diagram USB 3.0 OTG

3.3.5 PCIe M.2

The processor i.MX 8M Plus provides a PCIe Gen3 interface with one lane (x1). This is fully provided by the TQMa8MPxL in standard multiplexing. It is compatible with the PCI Express Base Specification, revision 3.0 and supports transfer rates of 2.5 GT/s as well as 5 GT/s.

For PCIe, the connection of a plug-in card in the M.2 form factor is provided. The M.2 standard defines different codings for the connector, an M.2 slot with "A+E" coding is used on the MBa8MPxL. M.2 modules are available in different form factors. The MBa8MPxL supports the common 2230 form factor.

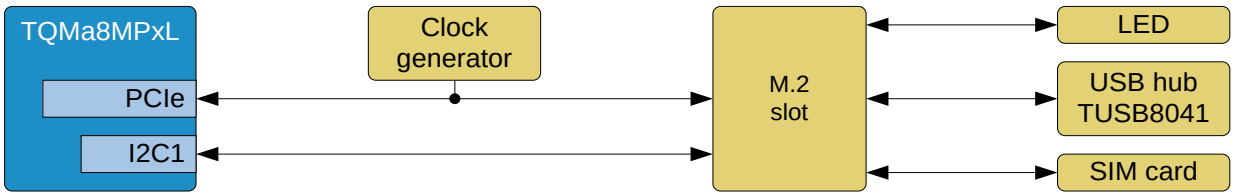

Figure 13: Block diagram PCIe M.2

As required by the M.2 specification, the motherboard's power budget provides 2 A for the plug-in card. The signals PERST0# and PEWAKE0# required for power mode control are connected to GPIOs of the CPU with 0 Ω resistors. CLKREQ0# on the other hand is connected to the input of the clock generator, which controls the clock channel of the M.2 card. The second input of the clock generator for the clock to the CPU is controlled by another GPIO.

Connected to the M.2 slot are the PCIe interface of the TQMa8MPxL, as well as a 3.3 V power supply. Furthermore, a USB host (from the USB hub) and an I2C interface are connected next to the PCIe lane. When using the I2C functionality, check in advance if the I2C address used by the plug-in card is not already used by a peripheral on the MBa8MPxL.

The reference clock for PCIe is provided by the external clock generator 9FGV0241. The clock generator can optionally be connected to the I2C bus with 0 Ω resistors. Via the I2C bus, individual outputs can be switched off and the slew rate and amplitude can be changed.

Any standard PCIe card can be used, provided that the necessary software drivers are available.

A micro SIM card holder is provided for the use of a GSM card. Since a combination of A-E-Key and B-Key is required for the proper use of a SIM card according to the standard, an unpopulated pin header is also provided. All signals required for the B-Key (pins 30, 32, 34, 36 and 66) are available on this, so customers can connect an adapter cable to a B-Key to it.

Table 10: Pinout SIM card connector, X46

Pin	Signal	Not
C1	V_UIM_PWR	Connected to pin 68 (UIM_POWER_SNK) of the M.2 slot
C2	UIM_RST	Connected to pin 1 of header X557
C3	UIM_CLK	Connected to pin 2 of header X557
C4	(NC)	–
C5	GND	–
C6	UIM_SWP	Connected to pin 66 (UIM_SWP) of the M.2 slot
C7	UIM_DATA	Connected to pin 3 of header X557
C8	(NC)	–
DC	SIM_DETECT	Connected to pin 5 of header X557
DS	GND	–

3.3.5 PCIe M.2 (continued)

Table 11: Pinout M.2, X48

Pin	Pin name	Target pin/net	Pin	Pin name	Target pin/net
75	GND	GND	M1/M2	M1; M2	GND
73	REFCLK-1/RSV	NC	74	3V3	V_3V3_PCIE
71	REFCLK+1/RSV	NC	72	3V3	V_3V3_PCIE
69	GND	GND	70	UIM_POWER_SRC	X557 – Pin 4
67	PER-1/RSV	NC	68	UIM_POWER_SNK	X46 – Pin C1
65	PER+1/RSV	NC	66	UIM_SWP	X46 – Pin C6
63	GND	GND	64	RSV	NC
61	PET-1/RSV	NC	62	ALERT#	NC
59	PET+1/RSV	NC	60	I2C_CLK	I2C_SCL_1V8
57	GND	GND	58	I2C_DATA	I2C_SDA_1V8
55	PEWAKE0#	GPIO2_IO11	56	W_DISABLE1#	V_3V3_PCIE
53	CLKREQ0#	PCIE_CLKREQ_CLK	54	W_DISABLE2#	V_3V3_PCIE
51	GND	GND	52	PERST0#	GPIO2_IO07
49	REFCLK-0	PCIE0_REFCLK_N	50	SUSCLK	G9
47	REFCLK+0	PCIE0_REFCLK_P	48	COEX_RXD	NC
45	GND	GND	46	COEX_TXD	NC
43	PER-0	PCIE_RXN	44	COEX3	NC
41	PER+0	PCIE_RXP	42	NC	NC
39	GND	GND	40	NC	NC
37	PET-0	PCIE_TXN	38	NC	NC
35	PET+0	PCIE_TXP	36	UART_RTS	NC
33	GND	GND	34	UART_CTS	NC
Mechanical Key (E-Key)			32	UART_TXD	NC
Mechanical Key (E-Key)					
23	SDIO_RESET#	NC		Mechanical Key (E-Key)	
21	SDIO_WAKE#	NC	22	UART_RXD	NC
19	SDIO_DATA3	NC	20	UART_WAKE#	NC
17	SDIO_DATA2	NC	18	GND	GND
Mechanical Key (A-Key)			16	LED2#	LED V181
Mechanical Key (A-Key)					
7	GND	GND	Mechanical Key (A-Key)		
5	USB_D-	USB30_H3_DN	6	LED1#	LED V132
3	USB_D+	USB30_H3_DP	4	3V3	V_3V3_MB
1	GND	GND	2	3V3	V_3V3_MB

3.3.6 Debug UART

For debug functionalities UART3 and UART4 are provided as virtual COM ports via USB. In parallel UART1 and UART2 are available at pin headers.

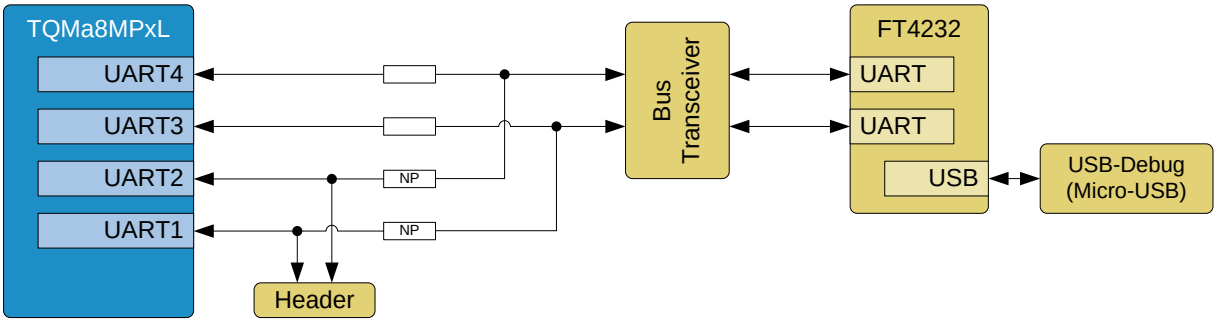

Figure 14: Block diagram UARTs

The FT4232 is bus-powered so that the COM port on the PC side is maintained even if the mainboard power supply is interrupted. The pinout of all UARTs is shown in Table 22, Pinout header X61.

3.3.7 MIPI DSI / DisplayPort

The TQMa8MPxL MIPI DSI interface, consisting of a differential clock signal and four differential data lines, is routed on the MBa8MPxL to DisplayPort connector X65 via a Toshiba TC9595XBG DSI-to-DisplayPort bridge.

The bridge supports DisplayPort 1.1a standard and thus resolutions of 1920x1200 at 60 FPS.

3.3 V is available at the DisplayPort connector, which can supply a maximum of 500 mA. This current must be subtracted from the current budget of the LM25119.

The TC9595's reference clock is generated by a 26 MHz oscillator, which is connected to the REFCLK input.

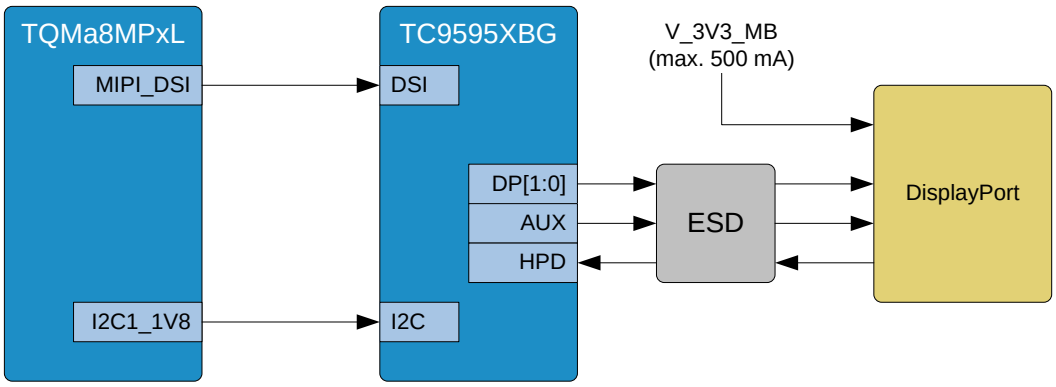

Figure 15: Block diagram DisplayPort

Table 12: Pinout DisplayPort, X65

Pin	Signal	Remark
1	DP_ML0+	–
2	DGND	–
3	DP_ML0–	–
4	DP_ML1+	–
5	DGND	–
6	DP_ML1–	–
7	(NC)	–
8	DGND	–
9	(NC)	–
10	(NC)	–
11	DGND	–
12	(NC)	–
13	DP_CFG1	1 MΩ termination
14	DP_CFG2	1 MΩ termination
15	DP_AUX_CH+	100 kΩ PD
16	DGND	–
17	DP_AUX_CH–	100 kΩ PU to 3.3 V
18	DP_HPD	100 kΩ PD; GPIO0 at DP bridge
19	DGND	–
20	V_3V3_DP	Max. 500 mA
M1…4	Shield / DGND	–

3.3.8 MIPI CSI

Both MIPI CSI interfaces provided by the TQMa8MPxL are routed to connector X57 on the bottom of the MBa8MPxL.

With a single camera, up to 4k at 45 FPS are supported, when using two cameras, the support splits to 1080p at 80 fps each.

Both CSI interfaces provide an I²C bus, four GPIO signals (reset, power enable, trigger, sync) and a master clock output on the connector.

The GPIO signals of the CSI0 interface are connected to the ECSPI1 signals, which are multiplexed as GPIO for this purpose. The GPIO signals of CSI1 are not connected by default due to missing software support. Instead, the ECSPI2 interface is provided on a pin header. If a use as GPIO is required, this can be made possible by equipping 0 Ω resistors.

The I²C buses operate at 1.8 V and are connected to I2C4 via a level shifter on the MBa8MPxL. CSI0 can optionally be connected to another I²C bus to avoid address conflicts.

The master clock signals can be connected to the Clock Control Module of the i.MX 8M Plus. Via this Clock Control Module both CSIs can be supplied with a reference clock each. The 0 Ω bridge for the connection is not assembled by default.

5 V are provided at pins 56, 58 and 60. This voltage may be loaded with a maximum of 300 mA.

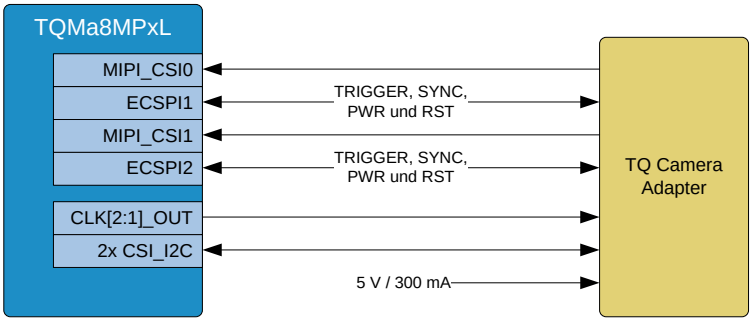

Figure 16: Block diagram MIPI CSI

Table 13: Pinout MIPI CSI, X57

Remark	Signal	Pin		Signal	Remark
–	GND	1	2	GND	–
10 kΩ PD	MIPI_CSI0_EN	3	4	MIPI_CSI1_EN	(NC), 10 kΩ PD
10 kΩ PD	MIPI_CSI0_RST#	5	6	MIPI_CSI1_RST#	(NC), 10 kΩ PD
–	MIPI_CSI0_TRIGGER	7	8	MIPI_CSI1_TRIGGER	(NC)
–	MIPI_CSI0_SYNC	9	10	MIPI_CSI1_SYNC	(NC)
–	(NC)	11	12	(NC)	–
–	GND	13	14	GND	–
–	MIPI_CSI0_DATA[3]_N	15	16	MIPI_CSI1_DATA[3]_N	–
–	MIPI_CSI0_DATA[3]_P	17	18	MIPI_CSI1_DATA[3]_P	–
–	GND	19	20	GND	–
–	MIPI_CSI0_DATA[2]_N	21	22	MIPI_CSI1_DATA[2]_N	–
–	MIPI_CSI0_DATA[2]_P	23	24	MIPI_CSI1_DATA[2]_P	–
–	GND	25	26	GND	–
–	MIPI_CSI0_DATA[1]_N	27	28	MIPI_CSI1_DATA[1]_N	–
–	MIPI_CSI0_DATA[1]_P	29	30	MIPI_CSI1_DATA[1]_P	–
–	GND	31	32	GND	–
–	MIPI_CSI0_DATA[0]_N	33	34	MIPI_CSI1_DATA[0]_N	–
–	MIPI_CSI0_DATA[0]_P	35	36	MIPI_CSI1_DATA[0]_P	–
–	GND	37	38	GND	–
–	MIPI_CSI0_CLK_N	39	40	MIPI_CSI1_CLK_N	–
–	MIPI_CSI0_CLK_P	41	42	MIPI_CSI1_CLK_P	–
–	GND	43	44	GND	–
Optional I2C_SDA_1V8	MIPI_CSI0_SDA	45	46	MIPI_CSI1_SDA	–
Optional I2C_SCL_1V8	MIPI_CSI0_SCL	47	48	MIPI_CSI1_SCL	–
–	GND	49	50	GND	–
0 Ω in series; (NP)	MIPI_CSI0_MCLK_OUT	51	52	MIPI_CSI1_MCLK_OUT	0 Ω in series; (NP); routed to TP243
–	GND	53	54	GND	–
–	(NC)	55	56	V_5V_SW	Max. 300 mA
–	(NC)	57	58		
–	(NC)	59	60		

3.3.9 LVDS

The i.MX 8M Plus offers an LVDS controller with a dual LVDS interface. Each of the interfaces uses four differential lanes.
On the MBa8MPxL there is one interface for connecting single or dual LVDS. In addition, two GPIO (BLT_EN, RESET#), a PWR_EN and a PWM signal are provided. GPIO3_IO14, GPIO3_IO19, GPIO3_IO20 and GPIO3_IO21 are used for these four 1.8 V signals.
If required, the signal PWM2 can be multiplexed on the same CPU pin instead of GPIO3_IO21.
Both DF19 LVDS connectors - Data and CMD - are placed on the bottom side of the MBa8MPxL.
The USB signals of the CMD connector are connected to port 4 of the USB 3.0 hub.

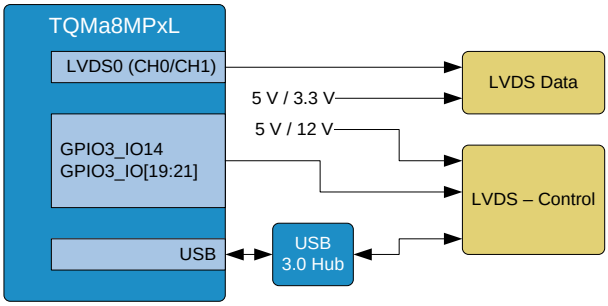

Figure 17: Block diagram LVDS

Table 14: Pinout LVDS data, X11

Pin	Signal
1	LVDS0_CH0_TX0_N
2	LVDS0_CH0_TX0_P
3	LVDS0_CH0_TX1_N
4	LVDS0_CH0_TX1_P
5	LVDS0_CH0_TX2_N
6	LVDS0_CH0_TX2_P
7	GND
8	LVDS0_CH0_CLOCK_N
9	LVDS0_CH0_CLOCK_P
10	LVDS0_CH0_TX3_N
11	LVDS0_CH0_TX3_P
12	LVDS0_CH1_TX0_N
13	LVDS0_CH1_TX0_P
14	GND
15	LVDS0_CH1_TX1_N
16	LVDS0_CH1_TX1_P
17	GND
18	LVDS0_CH1_TX2_N
19	LVDS0_CH1_TX2_P
20	LVDS0_CH1_CLOCK_N
21	LVDS0_CH1_CLOCK_P
22	LVDS0_CH1_TX3_N
23	LVDS0_CH1_TX3_P
24	GND
25	V_5V_LVDS0
26	
27	
28	V_3V3_LVDS0
29	
30	

Table 15: Pinout LVDS control, X7

Pin	Signal
1	12 V
2	
3	
4	DGND
5	
6	
7	5 V
8	
9	DGND
10	
11	V_VBUS30_H4
12	DGND
13	USB30_H4_DN
14	USB30_H4_DP
15	DGND
16	LVDS0_RESET#, 10 kΩ PD
17	LVDS0_BLT_EN, 10 kΩ PD
18	LVDS0_PWR_EN, 10 kΩ PD
19	LVDS0_PWM
20	DGND

3.3.10 HDMI

The HDMI_TX interface of the TQMa8MPxL is provided on the MBa8MPxL on an HDMI connector. Between TQMa8MPxL and HDMI socket is a "HDMI signal conditioning chip", which converts the levels and provides ESD protection. The HDMI_ARC_N and HDMI_ARC_P signals have capacitors between the module and the connector according to the EARC specification.

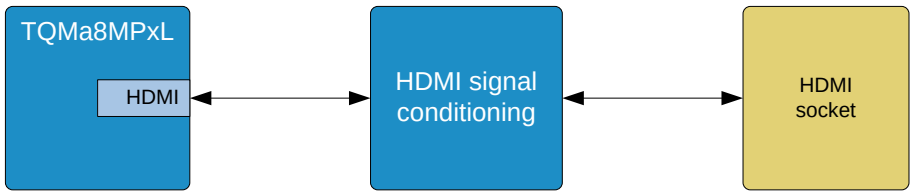

Figure 18: Block diagram HDMI

Table 16: Pinout HDMI connector, X44

Pin	Signal	Remark
1	HDMI_DATA2_P	–
2	GND	–
3	HDMI_DATA2_N	–
4	HDMI_DATA1_P	–
5	GND	–
6	HDMI_DATA1_N	–
7	HDMI_DATA0_P	–
8	GND	–
9	HDMI_DATA0_N	–
10	HDMI_CLK_P	–
11	GND	–
12	HDMI_CLK_N	–
13	HDMI_CEC_IC	–
14	HDMI_ARC_P	–
15	HDMI_DDC_SCL	1.87 kΩ PU to HDMI_5V_OUT
16	HDMI_DDC_SDA	1.87 kΩ PU to HDMI_5V_OUT
17	GND	–
18	HDMI_5V_OUT	–
19	HDMI_ARC_N / HDMI_HPD	–
M1…M4	Shield/GND	–

3.3.11 CAN FD

The CAN ports of the TQMa8MPxL are available on the MBa8MPxL via level converters on the 3-pin connectors X18 and X19. Both interfaces are galvanically isolated with 1 kV. The CAN interfaces are not galvanically isolated from each other.
Both CAN interfaces can each be terminated with a DIP switch.

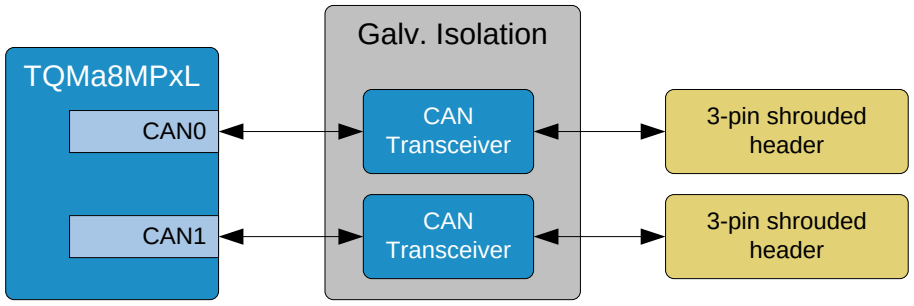

Figure 19: Block diagram CAN FD interface

Table 17: Pinout CAN FD connectors, X18, X19

Interface	Tub connector	Signal	Remark
CAN0	X18-1	CAN0_H	Galvanically isolated
	X18-2	CAN0_L	Galvanically isolated
	X18-3	GND_CAN	GND galvanically isolated
CAN1	X19-1	CAN0_H	Galvanically isolated
	X19-2	CAN0_L	Galvanically isolated
	X19-3	GND_CAN	GND galvanically isolated

3.3.12 Audio

A Texas Instruments TLV320 audio codec is assembled. It is configured via SAI3 and controlled by the I2C2 bus.
The audio codec provides microphone, line in and line out signals at 3.5 mm jacks on the MBa8MPxL.
The supply voltage and signal level operate at 1.8 V. All jack sockets are ESD protected.
Line out can become a headphone output by replacement of resistors R77/78 to R79/80.

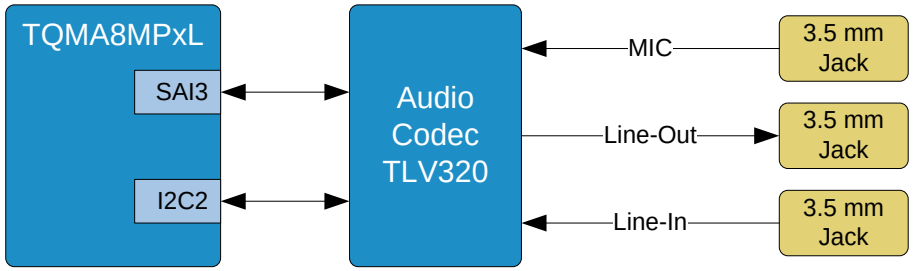

Figure 20: Block diagram audio interface

Table 18: Pinout audio connectors, X15, X16, X17

Jack	Pin	Signal	Remark
X15 MIC	1, 2	AGND_AUDIO	–
	4A, 4B	MIC_IN	2.4 kΩ in series to MIC_BIAS; ESD protection
	3	AGND_AUDIO	Right channel not used
X16 Line-In	1, 2	AGND_AUDIO	–
	4A, 4B	LINE_IN_L	ESD protection
	3	LINE_IN_R	ESD protection
X17 Line-Out	1, 2	AGND_AUDIO	–
	4A, 4B	AUDIO_OUT_L	ESD protection. Optional connection to HP_L
	3	AUDIO_OUT_R	ESD protection. Optional connection to HP_R

3.3.13 ECSPI

Up to three ECSPI interfaces are provided by the i.MX 8M Plus. These can be used on the MBa8MPxL for different interfaces. ECSPI3 is used for the ADC of the IO extension; see chapter 3.3.19. ECSPI1 and ECSPI2 are connected to pin headers as well as via 0 Ω bridges to the MIPI CSI connector. There they are used as GPIO control signals.

3.3.14 SPDIF

The SPDIF interface is not used as such on the MBa8MPxL, but can be provided on a pin header if required. By default these module signals are configured as GPIO to enable the control of the user LEDs via transistors.; see chapter 3.4.4.

3.3.15 GPT

The i.MX 8M Plus provides up to three general purpose timers. Signal GPT2_CLK is used to determine the fan speed.
The module signals GPT1_CLK and GPT1_CPTR2 are configured as GPIOs by default and are used to connect the two freely configurable buttons; see chapter 3.4.2. Alternatively, both signals can be connected to a pin header.
All three signals use I^2C or UART pins of the i.MX 8M Plus and have 3.3 V level.

3.3.16 PWM

The TQMa8MPxL provides two PWM signals, of which PWM3 is used to control the fan speed; see chapter 3.1.6.
PWM2 can be provided at pin GPIO3_IO21 and thus serve the PWM control of the LVDS display.

3.3.17 CCM

CLK1_IN and CLK2_IN of the Clock Control Module are routed on pin headers. CLK1_OUT and CLK2_OUT can be used as clock supply for the MIPI CSI interface. The 0 Ω bridge required for this is not equipped by default. All signals operate at 1.8 V.

3.3.18 TSE chip

For TQMa8MPxL variants with TSE chip, the corresponding circuitry is available for the pins used.

- The ISO 14443 interface is connected to a pin header where an antenna can be connected.
  If this TSE chip interface is not used, the signals are terminated with pull-down resistors.
- The ISO 7816 interface of the TSE chip is routed to a pin header; see chapter 3.3.20.
  If this TSE chip interface is not used, the signals are terminated according to the data sheet.

3.3.19 IO extension

The TQMa8MPxL provides eight GPIO1 interface pins as four outputs and four inputs at an IO connector on the MBa8MPxL.
All signals can operate at up to 24 V. The corresponding circuitry is provided on the MBa8MPxL.
The high-side switches, which supply the output signals, must be supplied with 24 V (max. 2 A) at pins B3 and B4. The supply voltage of 24 V provided at pins B1 and B2 can be used for this purpose.
Analog voltages are AD converted and transmitted to the ECSPI3 interface of the TQMa8MPxL.

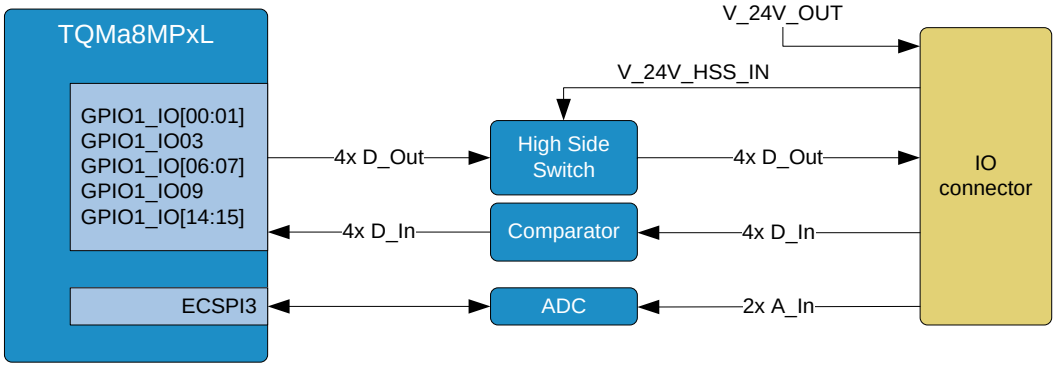

Figure 21: Block diagram IO extension

Table 19: Pinout IO extension connector, X555

Pin	Pin Name	Signal	Remark
B1	V_24V_OUT	V_24V_OUT	Loop-through supply voltage V_24V_IN
B2			
B3	V_24V_HSS_IN	V_24V_HSS_IN	Voltage supply for high-side switches (24 V ± 10 %)
B4			
B5	GND	GND	–
B6	D_OUT2	GPIO1_IO01	0 V to 24 V
B7	D_OUT1	GPIO1_IO00	
B8	D_OUT4	GPIO1_IO06	
B9	D_OUT3	GPIO1_IO03	
B10	D_IN1	GPIO1_IO07	
B11	D_IN2	GPIO1_IO09	
B12	D_IN3	GPIO1_IO14	
B13	D_IN4	GPIO1_IO15	
B14	ADC_IN1	ECSPI3	
B15	ADC_IN2	ECSPI3	
A1…A15	GND	GND	–

3.3.20 Pin header

All signals, which are not used on the MBa8MPxL are routed on two pin headers. Most of these signals can be configured as GPIO. 1.8 V, 3.3 V, and 5 V are available on each pin header.

Attention: Maximum current of 1.8 V, 3.3 V, and 5 V rails	
	The currents load of the 1.8V, 3.3 V and 5 V rails add up to the current consumption of the MBa8MPxL. The additional power required must be provided by the power supply of the MBa8MPxL. The maximum load of the fuse must be observed.

The maximum current load of the three voltage rails can be taken from the following table.

Table 20: Current load at pin headers

Voltage	I_{max}	Remark
1.8 V	0.75 A	Sum of currents at X61 and X63
3.3 V	1.75 A	Sum of currents at X11, X61, and X63
5 V	2.2 A	Sum of currents at X7, X11, X61, and X63

Signals with IO functionality are listed in the following table.
All complete listing of all available signals can be found in Table 22 and Table 23.

Table 21: Signals with IO functionality

CPU pin name	Signal	Alternative	Power group
USDHC1_DATA1	I2C6_SDA	GPIO2_IO03	V_SD1
USDHC1_DATA0	I2C6_SCL	GPIO2_IO02	V_SD1
USDHC1_CMD	UART1_RX	GPIO2_IO01	V_SD1
USDHC1_CLK	UART1_TX	GPIO2_IO00	V_SD1
USDHC1_DATA3	UART2_RX	GPIO2_IO05	V_SD1
USDHC1_DATA2	UART2_TX	GPIO2_IO04	V_SD1
GPIO1_IO05	M7_NMI	GPIO1_IO05	3.3 V
UART3_RXD	GPIO5_IO26	GPT1_CPTR2	3.3 V
UART3_TXD	GPIO5_IO27	GPT1_CLK	3.3 V
SPDIF_EXT_CLK	GPIO5_IO05	SPDIF_EXT_CLK	V_SAI2_SAI3
SPDIF_RX	GPIO5_IO04	SPDIF_IN	V_SAI2_SAI3
SPDIF_TX	GPIO5_IO03	SPDIF_OUT	V_SAI2_SAI3
SAI1_RXD0	ENET0_EVENT1_IN	GPIO4_IO02	1.8 V
SAI1_RXD1	ENET0_EVENT1_OUT	GPIO4_IO03	1.8 V
SAI2_TXD0	ENET1_EVENT2_IN	GPIO4_IO26	1.8 V
SAI2_RXD0	ENET1_EVENT2_OUT	GPIO4_IO23	1.8 V
ECSPI2_CS0	ECSPI2_CS0	GPIO5_IO13 or MIPI_CSI1_EN	1.8 V
ECSPI2_MISO	ECSPI2_MISO	GPIO5_IO12 or MIPI_CSI1_TRIGGER	1.8 V
ECSPI2_MOSI	ECSPI2_MOSI	GPIO5_IO11 or MIPI_CSI1_SYNC	1.8 V
ECSPI2_SCLK	ECSPI2_SCLK	GPIO5_IO10 or MIPI_CSI0_RST#	1.8 V

3.3.20 Pin header (continued)

Table 22: Pinout header X61

Dir.	Level	Group	Signal	Pin	Pin	Signal	Group	Level	Dir.
O	5 V	Power	V_5V_SW	1	2	V_1V8	Power	1.8 V	O
I	1.8 V	CCM	CLK1_IN	3	4	V_3V3_MB	Power	3.3 V	O
I	1.8 V	CCM	CLK2_IN	5	6	GND	Power	Ground	–
–	Ground	Power	GND	7	8	I2C6_SDA	SD	V_SD1	I/O
				9	10	I2C6_SCL	SD	V_SD1	O
I	V_SD1	SD	UART1_RX	11	12	GND	Power	Ground	–
O	V_SD1	SD	UART1_TX	13	14	PMIC_WDOG_IN#	TQMa8MPxL	3.3 V	I
–	Ground	Power	GND	15	16	GND	Power	Ground	–
I	V_SD1	SD	UART2_RX	17	18	QSPI1A_SCLK[1]	NAND	1.8 V	O
O	V_SD1	SD	UART2_TX	19	20	QSPI1A_DATA0[1]	NAND	1.8 V	I/O
–	Ground	Power	GND	21	22	QSPI1A_DATA1[1]	NAND	1.8 V	I/O
–	–	–	NC	23	24	QSPI1A_DATA2[1]	NAND	1.8 V	I/O
				25	26	QSPI1A_DATA3[1]	NAND	1.8 V	I/O
				27	28	QSPI1A_SS0#1	NAND	1.8 V	O
				29	30	GND	Power	Ground	–
				31	32	ISO_7816_CLK	TQMa8MPxL	3.3 V	I
–	Ground	Power	GND	33	34	ISO_7816_RST	TQMa8MPxL	3.3 V	I
I/O	V_SAI2_SAI3	GPIO	SPDIF_EXT_CLK[1]	35	36	ISO_7816_IO1	TQMa8MPxL	3.3 V	I/O
I	V_SAI2_SAI3	GPIO	SPDIF_IN[1]	37	38	ISO_7816_IO2	TQMa8MPxL	3.3 V	I/O
O	V_SAI2_SAI3	GPIO	SPDIF_OUT[1]	39	40	GND	Power	Ground	–

Table 23: Pinout header X63

Dir.	Level	Group	Signal	Pin	Pin	Signal	Group	Level	Dir.
O	5 V	Power	V_5V_SW	1	2	V_1V8	Power	1.8 V	O
–	Ground	Power	GND	3	4	V_3V3_MB	Power	3.3 V	O
I	1.8 V	ENET	ENET0_EVENT1_IN	5	6	GND	Power	Ground	–
O	1.8 V		ENET0_EVENT1_OUT	7	8	ECSPI2_CS0	ECSPI_HDMI	1.8 V	O
–	Ground	Power	GND	9	10	ECSPI2_MISO	ECSPI_HDMI	1.8 V	I/O
I	1.8 V	ENET	ENET1_EVENT2_IN	11	12	ECSPI2_MOSI	ECSPI_HDMI	1.8 V	O
O	1.8 V		ENET1_EVENT2_OUT	13	14	ECSPI2_SCLK	ECSPI_HDMI	1.8 V	O
–	Ground	Power	GND	15	16	GND	Power	Ground	–
				17	18	GPT1_CLK[1]	I2C_UART	3.3 V	I/O
I	3.3 V	GPIO	M7_NMI	19	20	GPT1_CPTR2[1]	I2C_UART	3.3 V	I

1 If 0 Ω bridges are placed, otherwise NC

3.4 Diagnostic and user interfaces

3.4.1 Boot Mode configuration

The Boot Mode is set with the 4-fold DIP switch S1 at the four i.MX 8M Plus pins Boot_Mode[3:0].
Information on the boot configuration of the i.MX 8M Plus can be found in the i.MX 8M Plus documentation; see Table 31.

Table 24: Boot Source options TQMa8MPxL

Boot Mode[3:0]	Boot Source
0 0 0 0	Boot from eFuses
0 0 0 1	USB Serial Downloader
0 0 1 0	Boot from eMMC (USDHC3)
0 0 1 1	Boot from SD card (USDHC2)
0 1 0 x	Boot from NAND (not supported)
0 1 1 0	Boot from QSPI (3-Byte Read)
0 1 1 1	Boot from Hyperflash 3.3 V (QSPI)
1 0 0 0	Boot from eCSPI (not supported)

3.4.2 Push buttons

On the MBa8MPxL two push buttons are routed to GPIOs via 0 Ω bridges. The signals between the push button and pin header have 10 kΩ pull-ups to 3.3 V. The push buttons switch to ground. (standard configuration as follows)

SWITCH_B# (S13) is connected with GPIO5_26
SWITCH_A# (S12) is connected with GPIO5_27

Alternatively, the GPIOs can be connected to a pin header (assembly option).

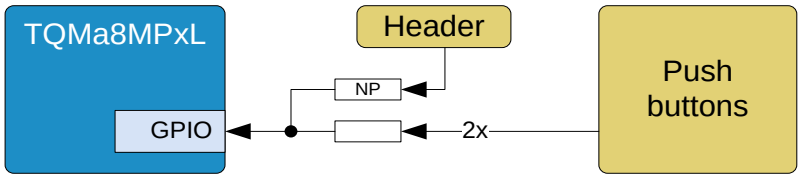

Figure 22: Block diagram pushbuttons

3.4.3 Reset button

More information can be found in chapter 3.1.7.

3.4.4 Status LEDs

The MBa8MPxL offers 21 diagnosis and status LEDs (plus the ones in the RJ45 connectors) to signal the system status.

Table 25: Status LEDs

Interface	Ref.	Colour	Indication
USB	V127	Green	Status V_VBUS30_H1 (lit when USB 3.0 port 1 is active)
	V128	Green	Status V_VBUS30_H2 (lit when USB 3.0 port 2 is active)
	V131	Green	Status V_VBUS_OTG (lit when USB 3.0 OTG is active)
USB debug	V143	Green	Status 3.3 V Debug (lit when 3.3 V for FTDI chip is active)
GPIO	V55	Green	Free LED, per light guide at front. Placement option: SPDIF_EXT_CLK
	V56	Green	Free LED, per light guide at front. Placement option: SPDIF_IN
	V60	Yellow	Free LED, per light guide at front. Placement option: SPDIF_OUT
Power	V3	Green	Status 24 V high-side switch (lit when high-side switch is active)
	V4	Green	Status 24 V MBa8MPxL (lit when 24 V for MBa8MPxL is active)
	V5	Green	Status 12 V MBa8MPxL (lit when 12 V for MBa8MPxL is active)
	V6	Green	Status 5 V MBa8MPxL (lit when 5 V for MBa8MPxL is active)
	V7	Green	Status 3.3 V MBa8MPxL (lit when 3.3 V for MBa8MPxL is active)
	V8	Green	Status 1.8 V MBa8MPxL (lit when 1.8 V for MBa8MPxL is active)
	V9	Green	Status 5 V TQMa8MPxL (lit when 5 V for TQMa8MPxL is active)
	V10	Orange	Status 3.3 V SD card (lit when 3.3 V for SD card is active)
	V11	Orange	Status 3.3 V TQMa8MPxL (lit when 3.3 V of TQMa8MPxL is active)
	V12	Orange	Status 1.8 V TQMa8MPxL (lit when 1.8 V of TQMa8MPxL is active)
LVDS	V111	Green	Indicator LED for LVDS interface
Reset	V59	Red	Reset LED, per light guide at front
PCIe (M.2)	V132	Green	Indicator LED for M.2 devices
	V181	Green	Indicator LED for M.2 devices
Ethernet	X66	–	See 3.3.1

3.4.5 GPIO

All GPIOs provided by the TQMa8MPxL are used as control signals on the MBa8MPxL and are therefore not available.
GPIOs can however be configured from signals available at the pin headers; see chapter 3.3.20.
A complete list of all possible GPIO pins can be found in the i.MX 8M Plus data sheet (1).

3.4.6 JTAG®

The JTAG® port of the i.MX 8M Plus is routed to a standard ARM® 10-pin JTAG® connector (X22) on the MBa8MPxL. JTAG_SRST# is connected to RESET_IN# via a buffer. The same reset can be executed as with reset button S7.
The JTAG® interface is not ESD protected.

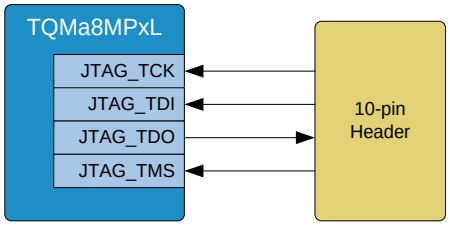

Figure 23: Block diagram JTAG

The following table shows the JTAG® connector pinout.

Table 26: Pinout JTAG® pin header, X22

Pin	Signal	Remark
1	V_{ref} / VCC	3.3 V, optional: 1.8 V
2	JTAG_TMS	10 kΩ PU, (NP)
3	GND	–
4	JTAG_TCK	10 kΩ PU, 10 kΩ PD, both (NP)
5	GND	–
6	JTAG_TDO	–
7	Key	(NC)
8	JTAG_TDI	10 kΩ PU, (NP)
9	GND_DETECT	10 kΩ PD
10	JTAG_SRST#	RESET_IN#, 10 kΩ PU

4. SOFTWARE

No software is required for the MBa8MPxL. Suitable software is only required on the TQMa8MPxL and is not a part of this User's Manual. More information can be found in the TQ-Support Wiki for the TQMa8MPxL.

5. MECHANICS

5.1 MBa8MPxL dimensions

The MBa8MPxL has overall dimensions (length × width) of 160 × 100 mm².
The highest component on the top side of the MBa8MPxL is approximately 15.5 mm (stacked USB Type A connector).
The highest component on the bottom side of the MBa8MPxL is approximately 12 mm (pin header).
The overall height of the MBa8MPxL is approximately 29 mm.
The TQMa8MPxL assembled on the MBa8MPxL has a height of 3.18 mm ±0.23 mm above the MBa8MPxL.
The MBa8MPxL provides four 3.2 mm housing mounting holes, and four 2.7 mm heat sink mounting holes.
The MBa8MPxL including TQMa8MPxL weighs approximately 143 grams.

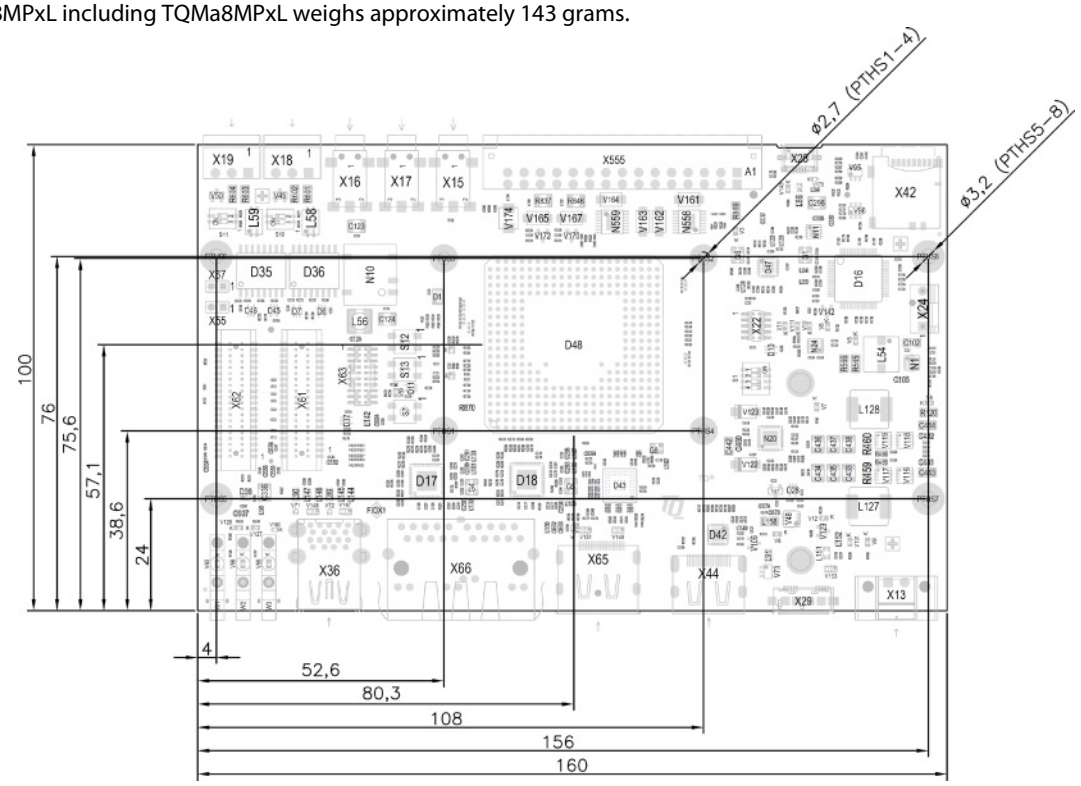

Figure 24: MBa8MPxL dimensions

5.2 Embedding in the overall system

The MBa8MPxL serves as a design base for customer products, as well as a platform to support during development.

5.3 Housing

The form factor and the mounting holes of the MBa8MPxL are designed for installation in a standard EURO housing.

5.4 Thermal management

The combination of MBa8MPxL and TQMa8MPxL has a power consumption of approximately 5 to 6 watts.
Further power consumption occurs mainly at externally connected devices.

Attention: TQMa8MPxL heat dissipation	
	The i.MX 8M Plus belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa8MPxL must be taken into consideration when connecting the heat sink. The TQMa8MPxL is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa8MPxL or the MBa8MPxL and thus malfunction, deterioration or destruction.

5.5 Assembly

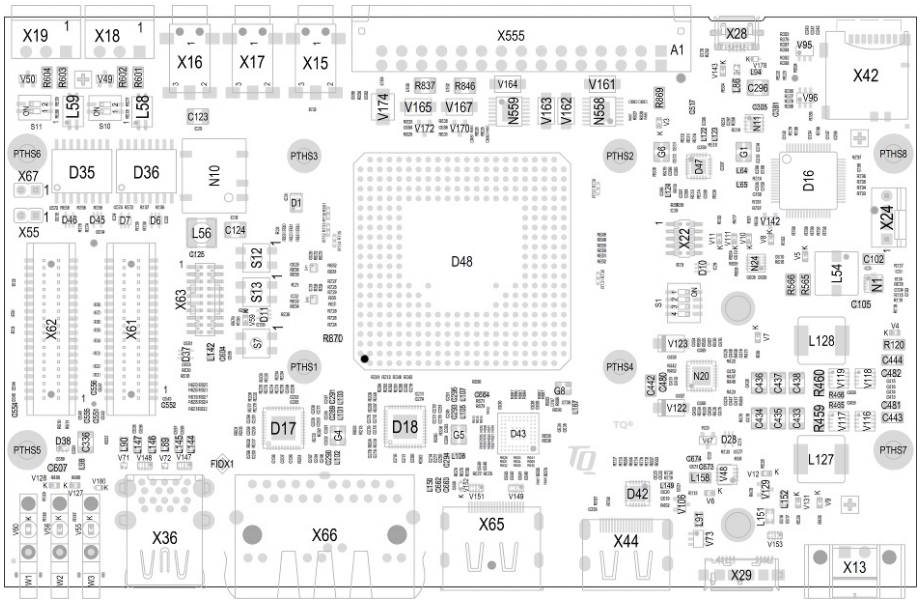

Figure 25: MBa8MPxL component placement top

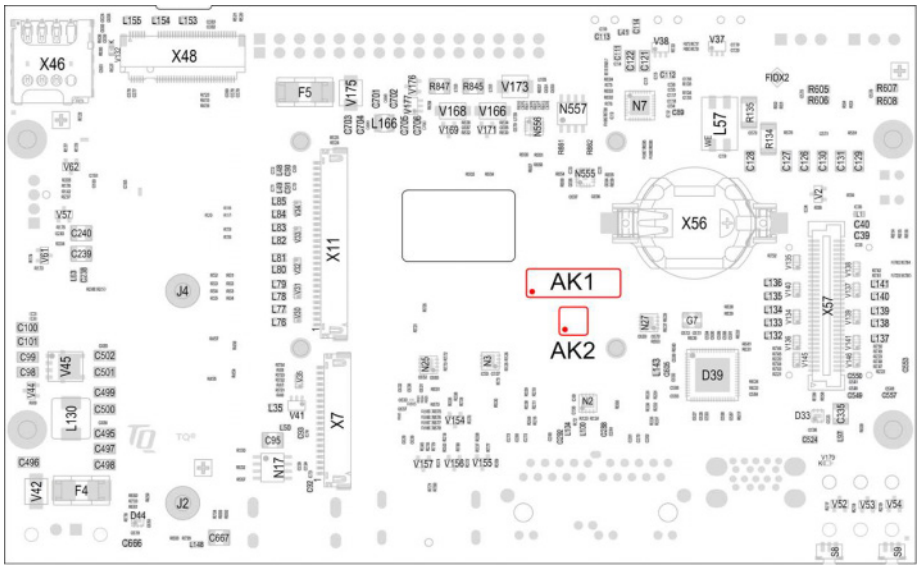

Figure 26: MBa8MPxL component placement bot

The labels on the MBa8MPxL show the following information:

Table 27: Labels on MBa8MPxL

Label	Content
AK1	MBa8MPxL version and revision, tests performed
AK2	Serial number

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Since the MBa8MPxL is a development platform, no EMC tests have been performed.

6.2 ESD

Most interfaces provide ESD protection. Details are to be taken from the MBa8MPxL schematics.

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤30 V DC.

6.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa95xxSA is only a sub-component of an overall system.

6.5 Intended Use

TQ DEVICES, PRODUCTS AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION IN NUCLEAR FACILITIES, AIRCRAFT OR OTHER TRANSPORTATION NAVIGATION OR COMMUNICATION SYSTEMS, AIR TRAFFIC CONTROL SYSTEMS, LIFE SUPPORT MACHINES, WEAPONS SYSTEMS, OR ANY OTHER EQUIPMENT OR APPLICATION REQUIRING FAIL-SAFE PERFORMANCE OR IN WHICH THE FAILURE OF TQ PRODUCTS COULD LEAD TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE. (COLLECTIVELY, "HIGH RISK APPLICATIONS")

You understand and agree that your use of TQ products or devices as a component in your applications are solely at your own risk. To minimize the risks associated with your products, devices and applications, you should take appropriate operational and design related protective measures.

You are solely responsible for complying with all legal, regulatory, safety and security requirements relating to your products. You are responsible for ensuring that your systems (and any TQ hardware or software components incorporated into your systems or products) comply with all applicable requirements. Unless otherwise explicitly stated in our product related documentation, TQ devices are not designed with fault tolerance capabilities or features and therefore cannot be considered as being designed, manufactured or otherwise set up to be compliant for any implementation or resale as a device in high risk applications. All application and safety information in this document (including application descriptions, suggested safety precautions, recommended TQ products or any other materials) is for reference only. Only trained personnel in a suitable work area are permitted to handle and operate TQ products and devices. Please follow the general IT security guidelines applicable to the country or location in which you intend to use the equipment.

6.6 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.7 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 28: Climatic and operational conditions MBa8MPxL

Parameter	Range	Remark
Ambient temperature	0 °C to +60 °C	With Lithium battery
Ambient temperature	0 °C to +70 °C	Without Lithium battery
Storage temperature	–10 °C to +60 °C	With Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMa8MPxL heat dissipation	
	The i.MX 8M Plus belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa8MPxL must be taken into consideration when connecting the heat sink. The TQMa8MPxL is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa8MPxL or the MBa8MPxL and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBa8MPxL. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa8MPxL.

The MBa8MPxL is designed to be insensitive to vibration and impact.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa8MPxL is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa8MPxL was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.
The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.
Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.
TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

8.5 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa8MPxL must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBa8MPxL enable compliance with EuP requirements for the MBa8MPxL.

8.6 Packaging

The MBa8MPxL is delivered in reusable packaging.

8.7 Batteries

8.7.1 General notes

Due to technical reasons a battery is necessary for the MBa8MPxL. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used. If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.7.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa8MPxL, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa8MPxL is minimised by suitable measures.
Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4

material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls). These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 29: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AI	Artificial Intelligence
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
CAN	Controller Area Network
CAN FD	Controller Area Network Flexible Data-Rate
CCM	Clock Control Module
CPU	Central Processing Unit
CSI	Camera Serial Interface
DIP	Dual In-line Package
DNC	Do Not Connect
DP	DisplayPort
DSI	Display Serial Interface
eCSPI	enhanced Capability Serial Peripheral Interface
eDP	embedded DisplayPort
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
ESD	Electrostatic Discharge
EU	European Union
EuP	Energy using Products
FPS	Frames Per Second
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GPT	General Purpose Timer
HD	High Density (graphics)
HDMI	High-Definition Multimedia Interface
HSS	High-Side Switch
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LPDDR4	Low-Power DDR4
LVDS	Low Voltage Differential Signal

9.1 Acronyms and definitions (continued)

Table 30: Acronyms (continued)

Acronym	Meaning
MAC	Media Access Controller
MIC	Microphone
MIPI	Mobile Industry Processor Interface
ML	Machine Learning
MTBF	Mean operating Time Between Failures
NAND	Not-And (flash memory)
NC	Not Connected
NMI	Non-Maskable Interrupt
NOR	Not-Or
NP	Not Placed
O	Output
OTG	On-The-Go
P	Power
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media-Independent Interface
RJ45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RPM	Revolutions Per Minute
RTC	Real-Time Clock
SAI	Serial Audio Interface
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SPDIF	Sony-Philips Digital Interface Format
SVHC	Substances of Very High Concern
TSE	Trust Secure Element
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra-High Speed
UM	User's Manual
UN	United Nations
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
WEEE®	Waste Electrical and Electronic Equipment
ZIF	Zero Insertion Force

9.2 References

Table 30: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	i.MX 8M Plus Applications Processor Data Sheet	Rev. 1 / 08/2021	NXP
(2)	i.MX 8M Plus Applications Processor Reference Manual	Rev. 1/ 03/2021	NXP
(3)	Mask Set Errata i.MX 8M Plus	– current –	NXP
(4)	TQMa8MPxL User's Manual	– current –	TQ-Systems
(5)	TQMa8MPxL Support Wiki	– current –	TQ-Systems

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